

TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-Memory, CPU-PEG/Display	3,4
CPU-Control/MISC/CFG/Audio	5
CPU-Power,CPU-GND	6,7
DDR4 DIMM1&DDR4 DIMM2	8,9,10,11
PCH-USB/PCIE/DMI/SATA	12
PCH-Audio/Display/Clock	13
PCH-GPIO/USB0C#/SATASTRAP	14
PCH-LPC/SPI/SMBUS/MISC	15
PCH-Power,PCH-GND,PCH-Strap	16,17,18
PCIE SLOT-CPU(X16)	19
PCIE SLOT-PCH(X1)	20
SATA	21
AUDIO - ALC887/depop circuit	22,23
LAN I219V	24
DVI/HDMI/VGA	25~27
M.2/USB2.0/USB3.0/PS2/SERIAL PORT	28~32
FAN/SIO-NUVOTON 5567/CLR_CMOS/BIOS ROM	33~37
GREEN PAK DEEP /ACPI CONTROLLER	38,39
PWM-RT3607BC/VCORE 4PHASE/VGT 2PHASE	40~42
DDR-RT8231/DDR-PM2143-VPP25	43,44
CPU PWR_ST/PLL/PCH Core power	45,46
VCCSA - POWER/VCCIO - POWER	47
ATX F_Panel/TPM/MSI_LED	48
DEBUG LED/JLED/EMI CAP/Manial Part	49~53

MS-7B28

ATX:230mm*185mm

Intel -CoffeeLake-S plamform

CPU:

LGA1151

CPU POWER PAK *4Phase

GT POWER PAK *2 Phase

Onboard Chip:

SIO: NUVOTON 5567

HD Audio Codec: ALC887

LAN: INTEL I219V

Flash ROM: SPI 64 MB

CUT VBAT:SLG4B41231

Main Memory:

DDR4 * 2 (Dual Channel)

ACPI:

5VDAUL:uP7501

5VDIMM:uP7501

3VSB:GS7133+N MOS

1P8_VSB:GS7166

3VDSW:L11831

VCCSTPLL:GS7133

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

System Chipset:

H310

PWM:

VCORE - RT3607	138A
VGT- RT3607	45A
DDR - RT8231	11.525A
DDR VPP25- MP2143	1.12A
PCH(1.05V) - RT8125E	10.743A
VCCSA - RT8125E	11.1A
VCCIO - SY8288	6.4A

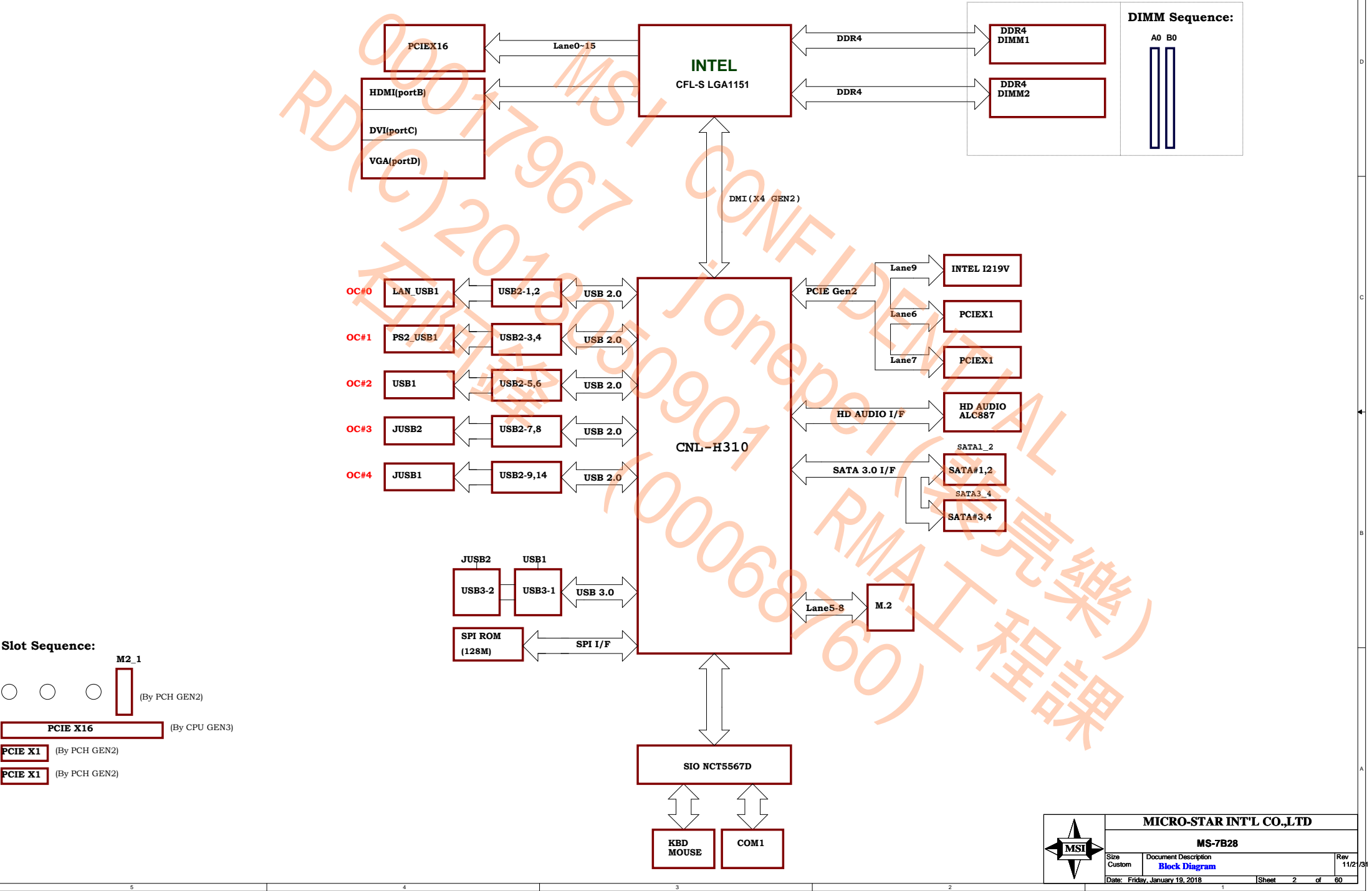


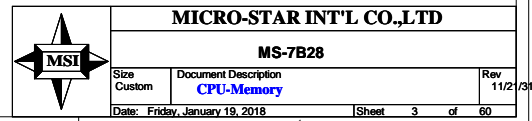
MICRO-STAR INT'L CO.,LTD

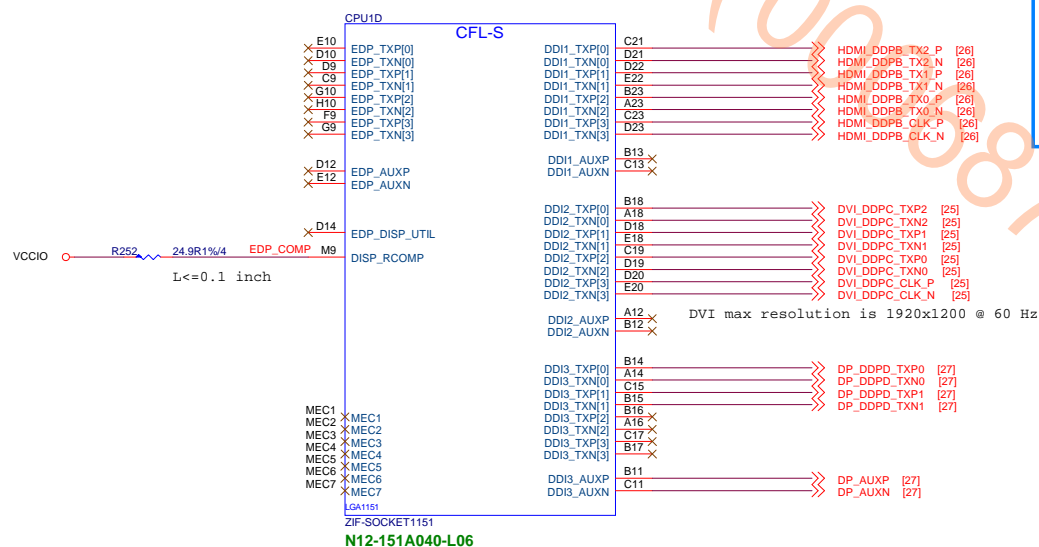
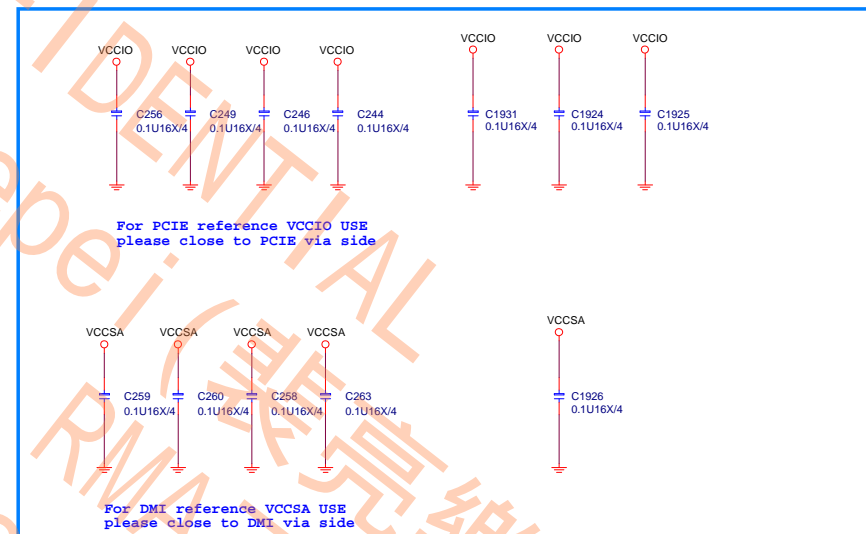
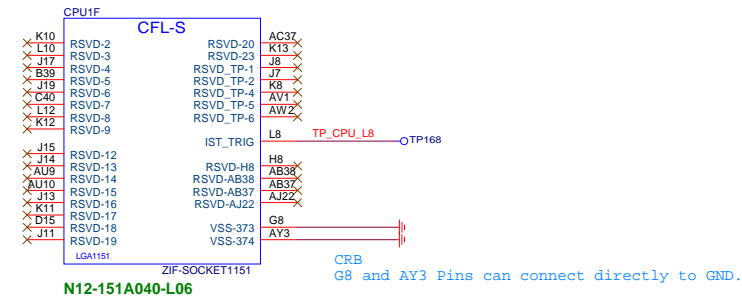
MS-7B28

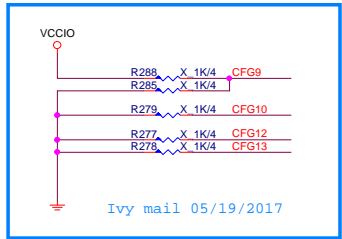
Size Custom	Document Description Cover Sheet	Rev 11/2
Date: Friday, January 19, 2018	Sheet 1 of 60	

Block Diagram

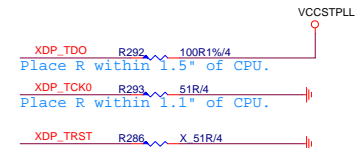
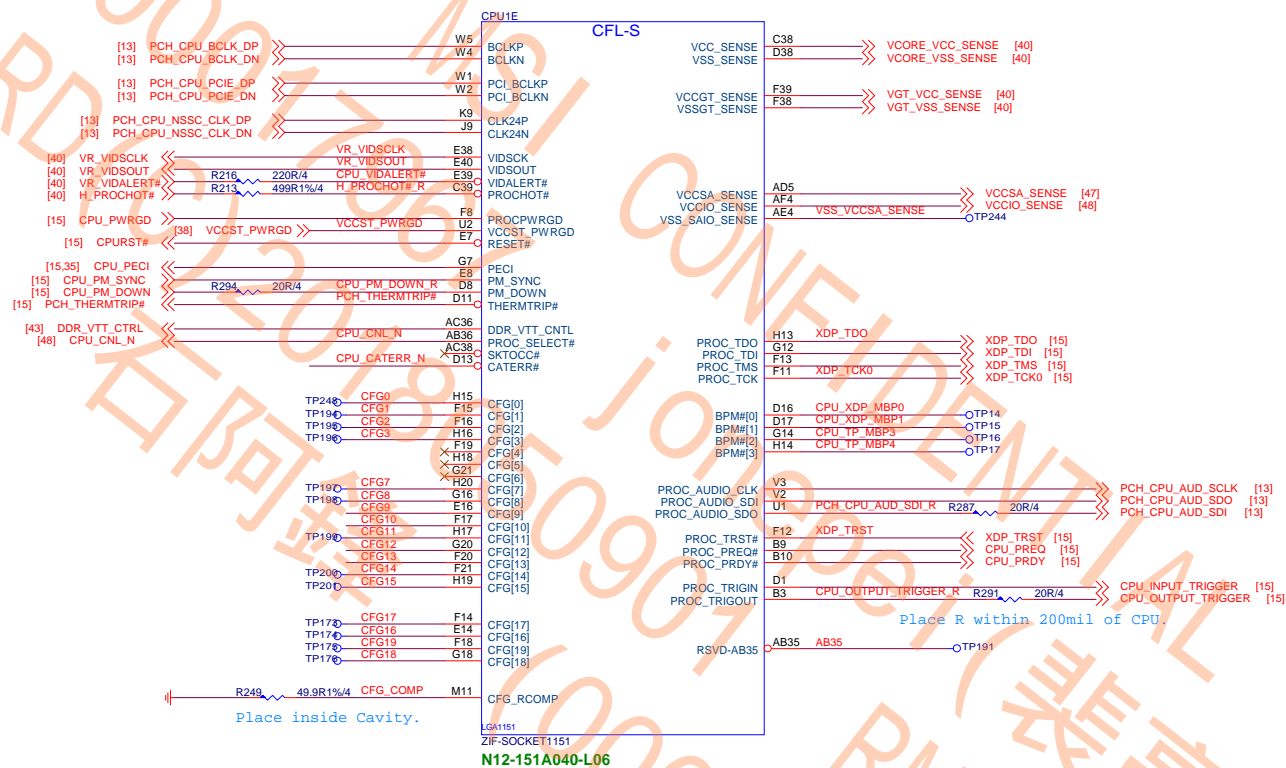
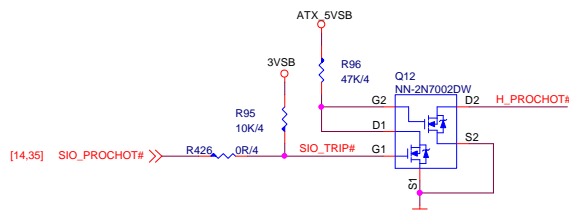






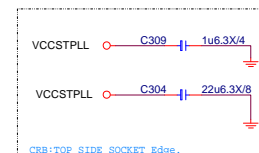
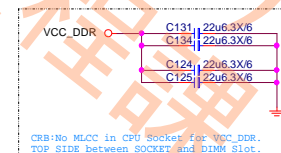
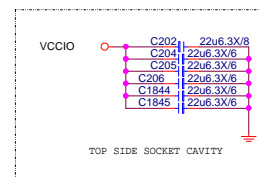
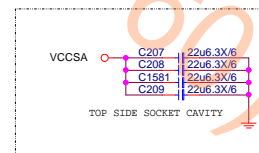
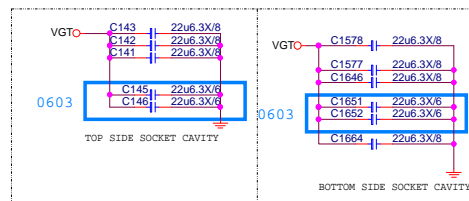
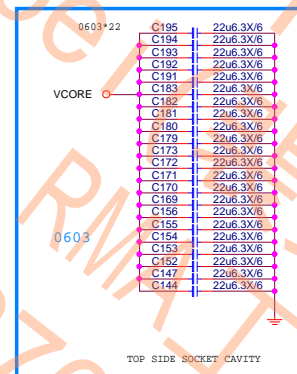
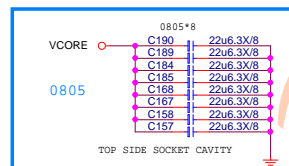
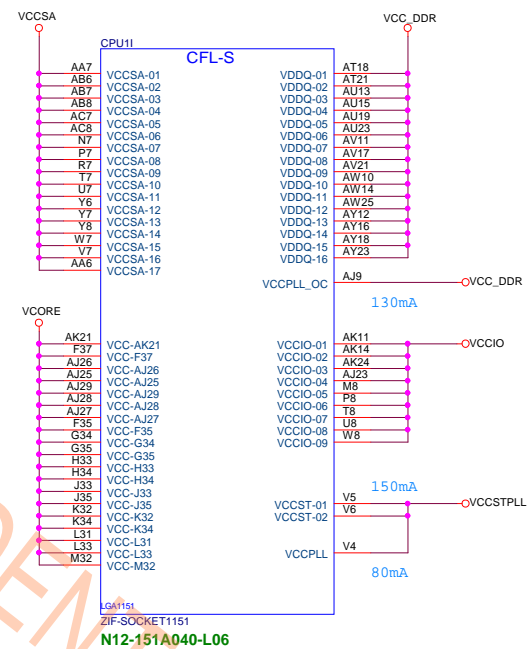
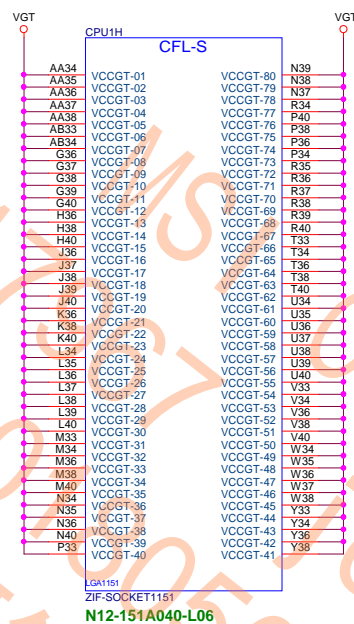
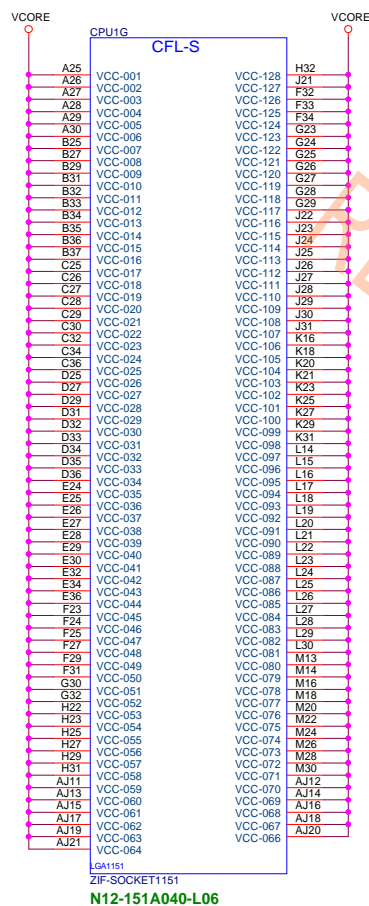


CFG Table			
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCI Bus Lock
1			RSVD
2	NORM	REVERSE	PG. LANE REVERSAL
3	DISABLE	ENABLE	oPp
5	DISABLE	ENABLE	PG0CFGSEL[0]
6	DISABLE	ENABLE	PG0CFGSEL[1]
7	RESET#	RSTO REQ	PG. CAPS. TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14			RSVD
15			RSVD



MS-7B28

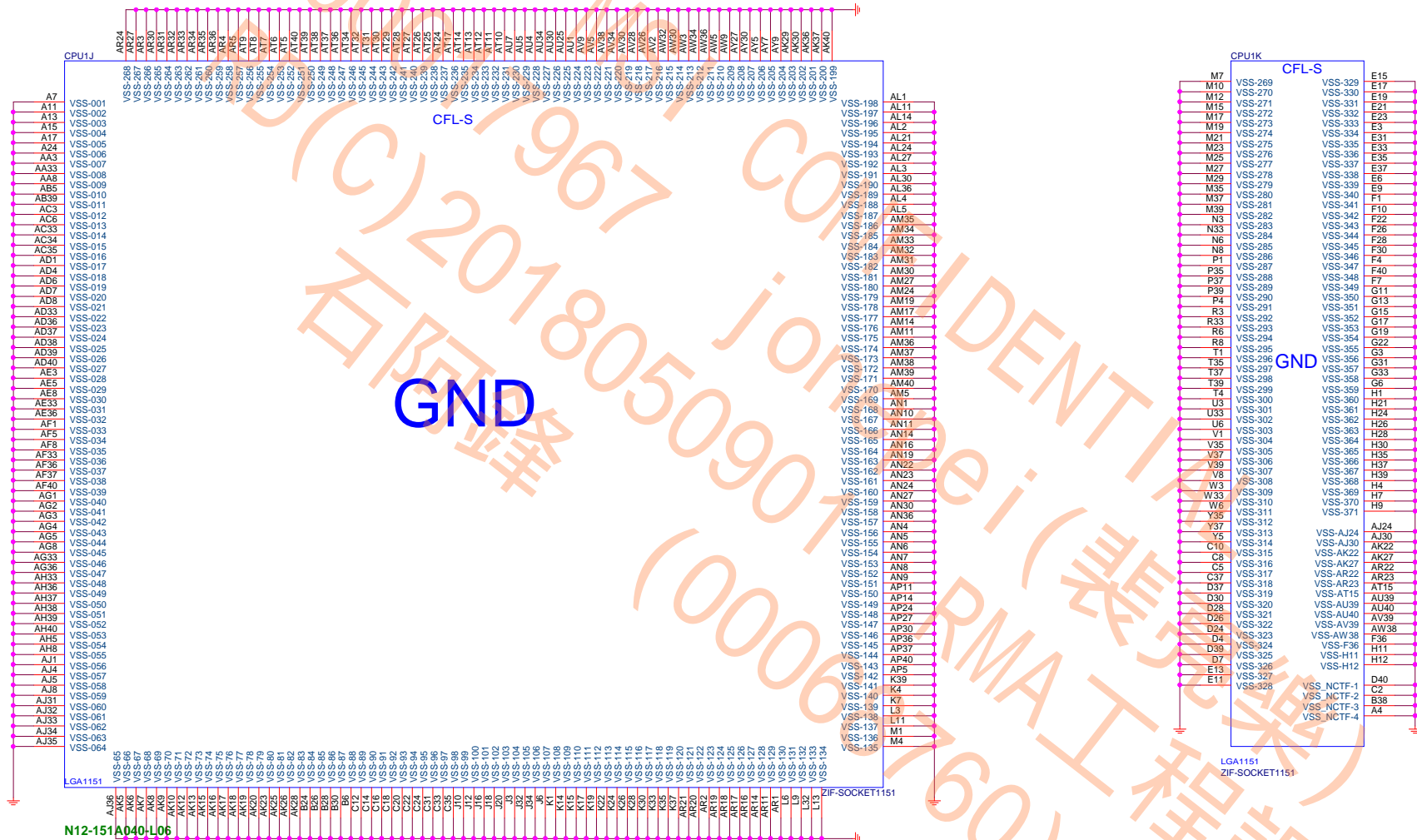
Size Custom	Document Description CPU-Control/MISC/CFG/Audio	Rev 11/2/3
Date: Friday, January 19, 2018		Sheet 5 of 60

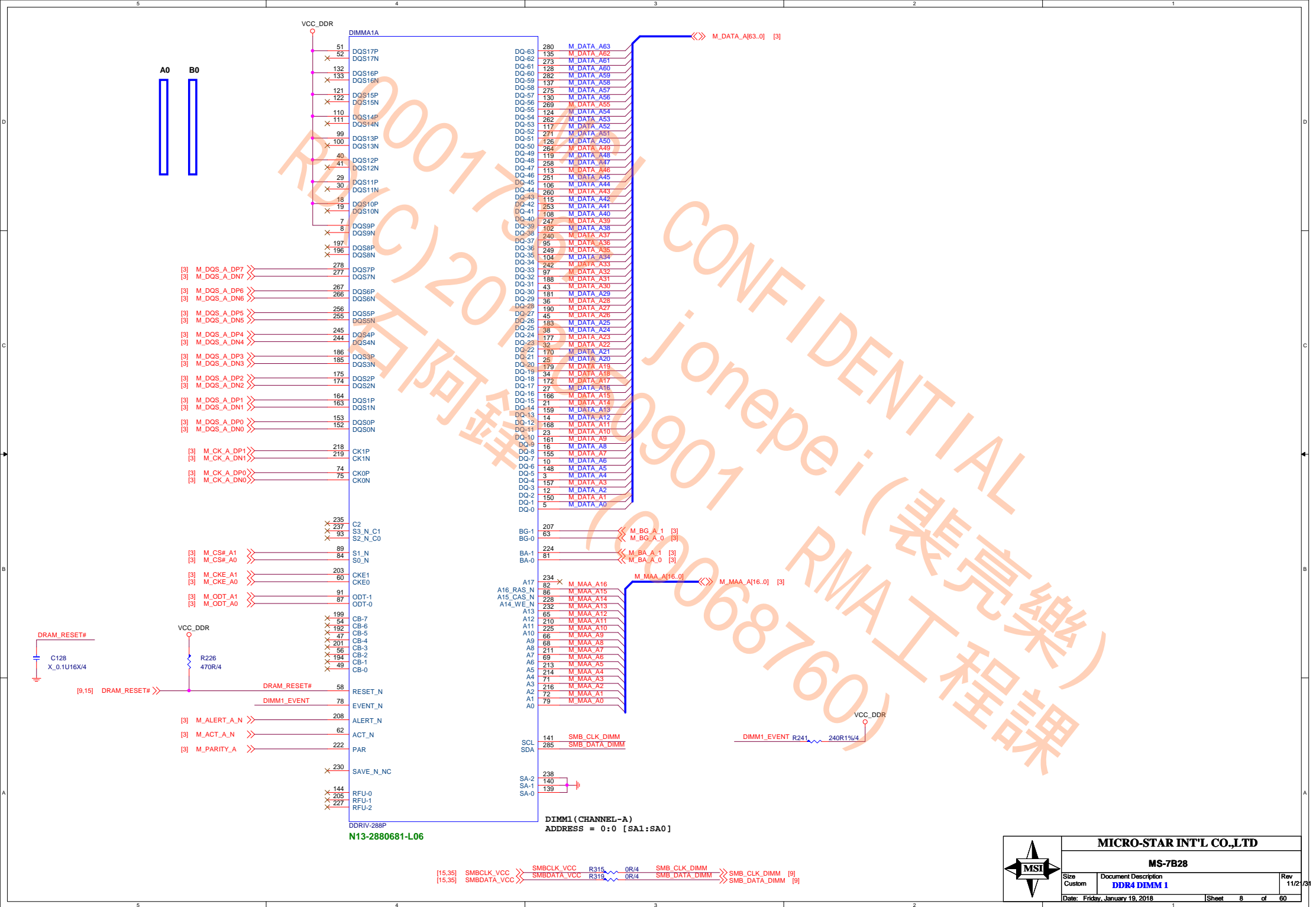


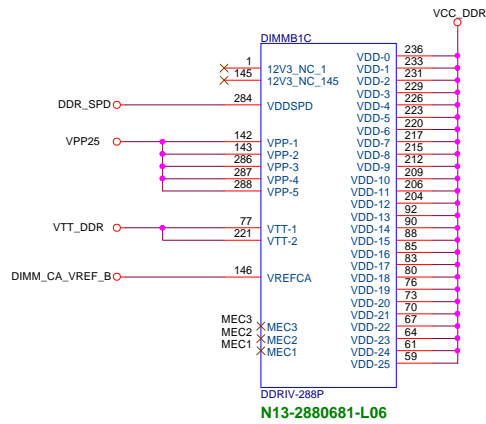
MICRO-STAR INT'L CO.,LTD

MS-7B28

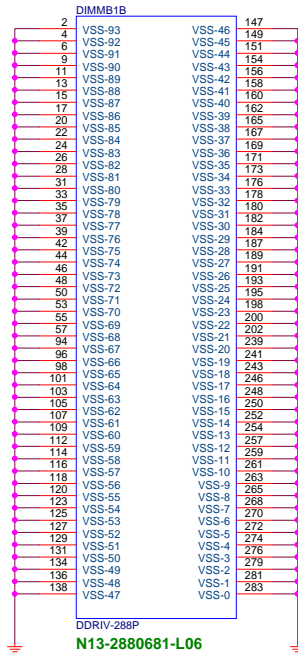
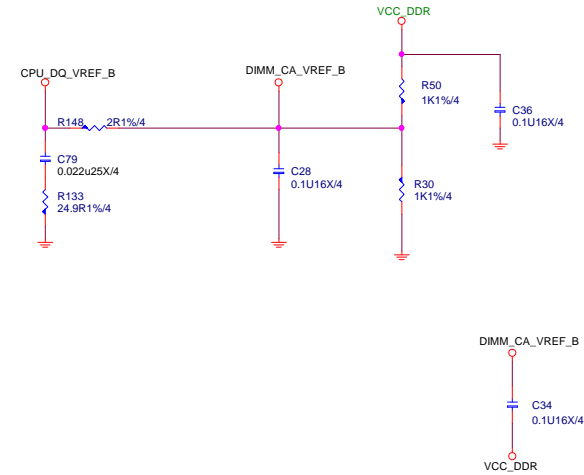
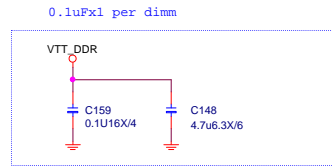
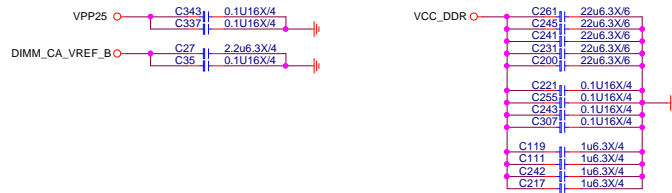
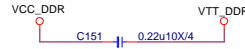
Size Custom	Document Description CPU-Power	Rev 11/2/3
Date: Friday, January 19, 2018		Sheet 6 of 60



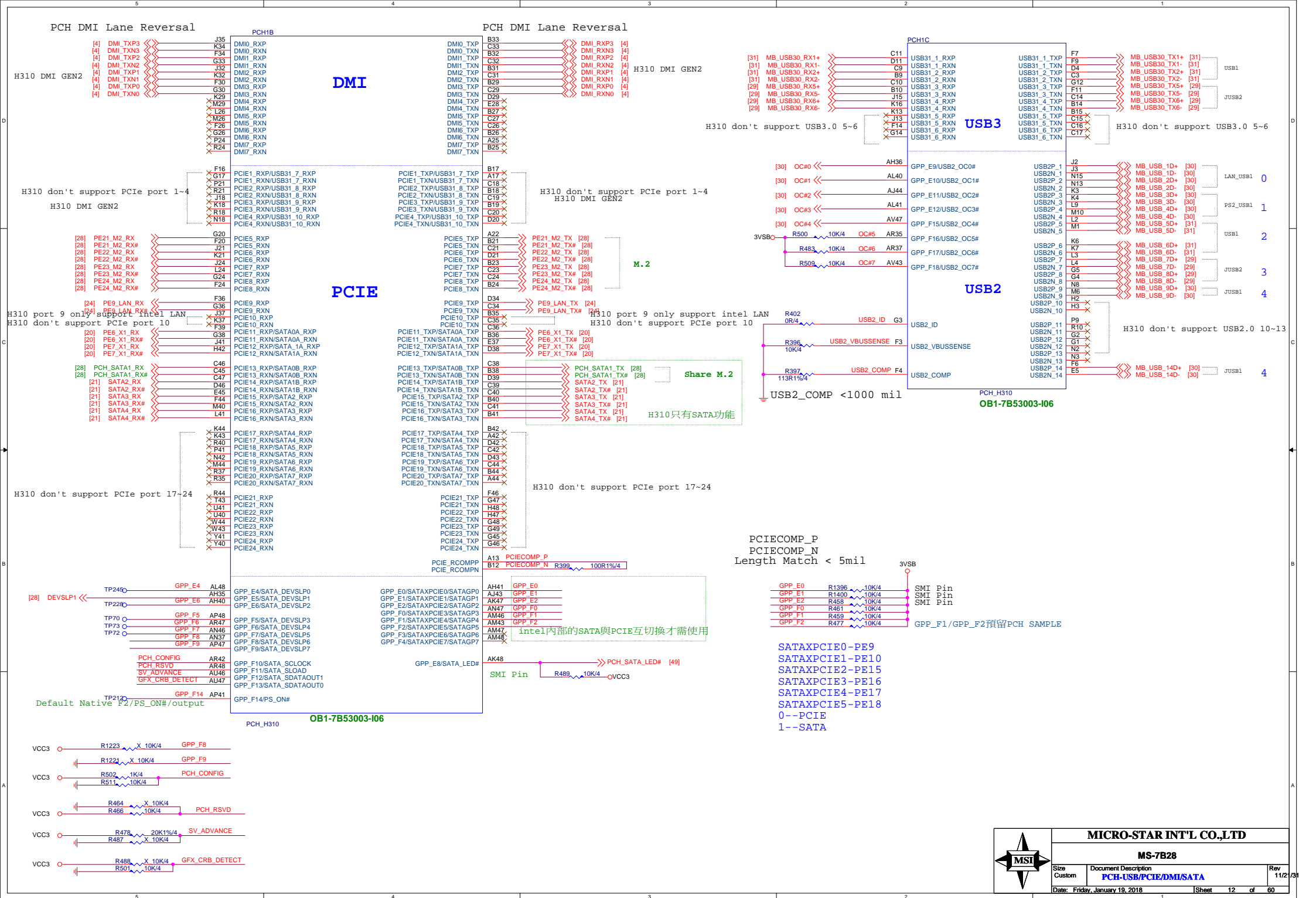




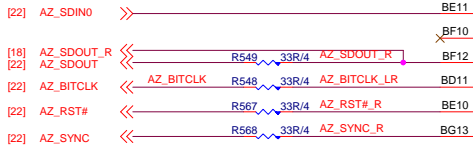
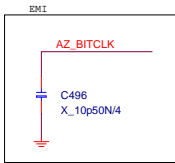
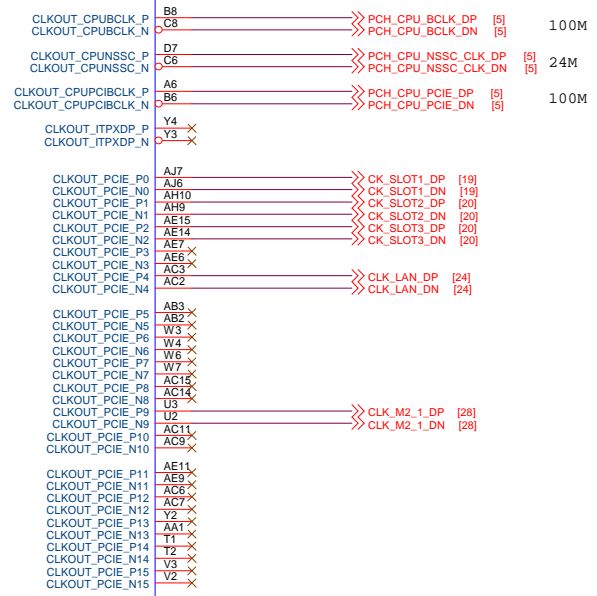
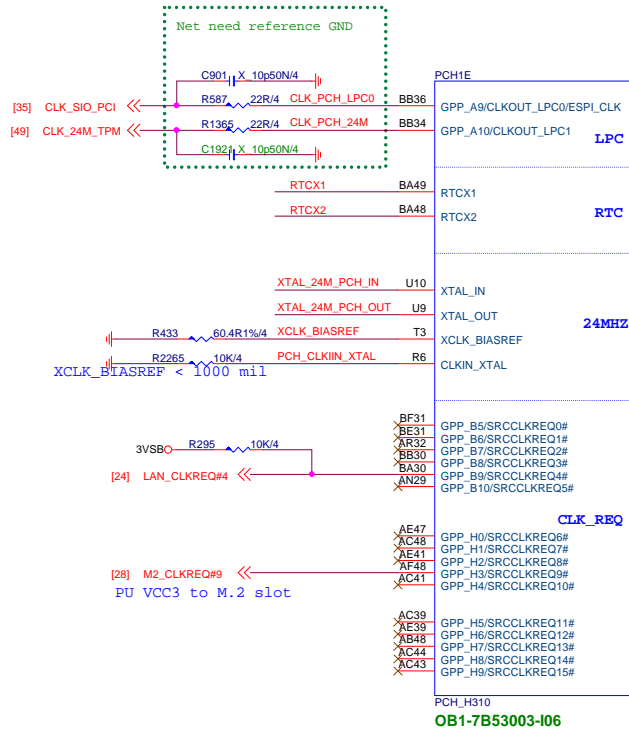
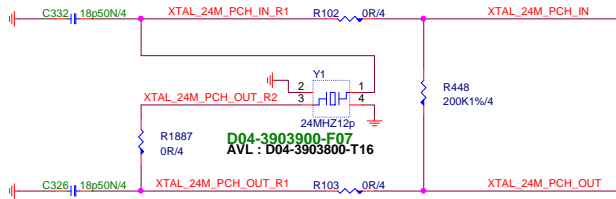
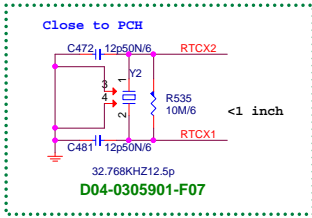
N13-2880681-L06



N13-2880681-L06

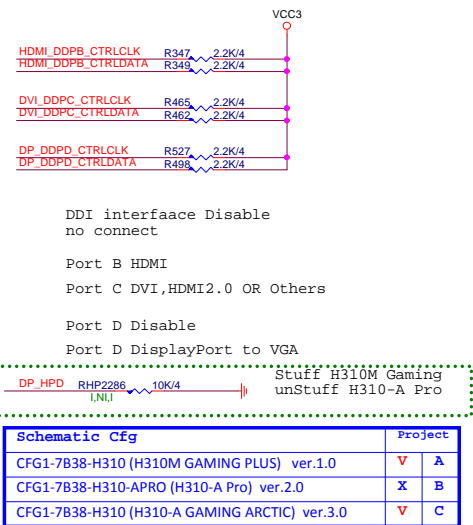
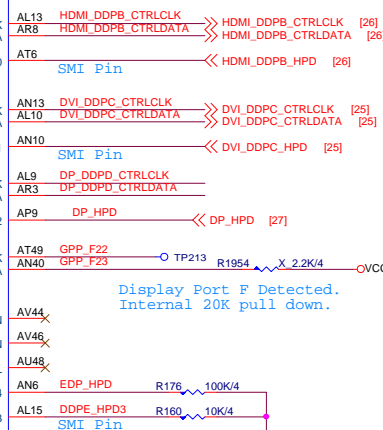
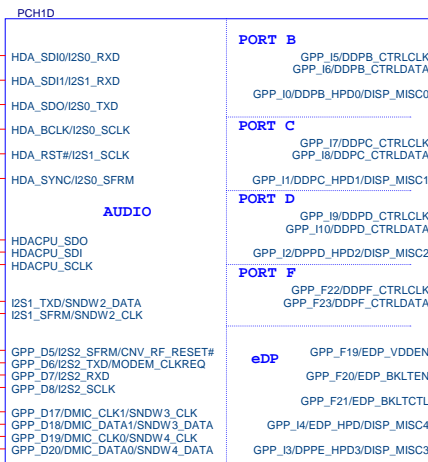


RTC Block

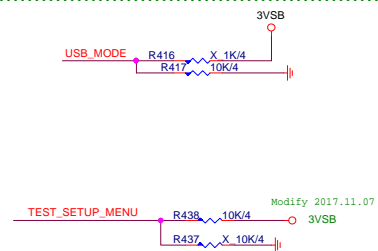
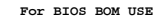
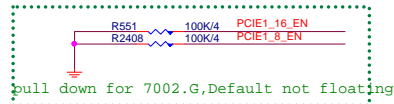


Default Native F3/CNV_RF_R_ESET#.

Default Native F3/MODEM_CLKREQ.



GPP_G[7:0] (Support SMI# only)



Modify 2017.11.07

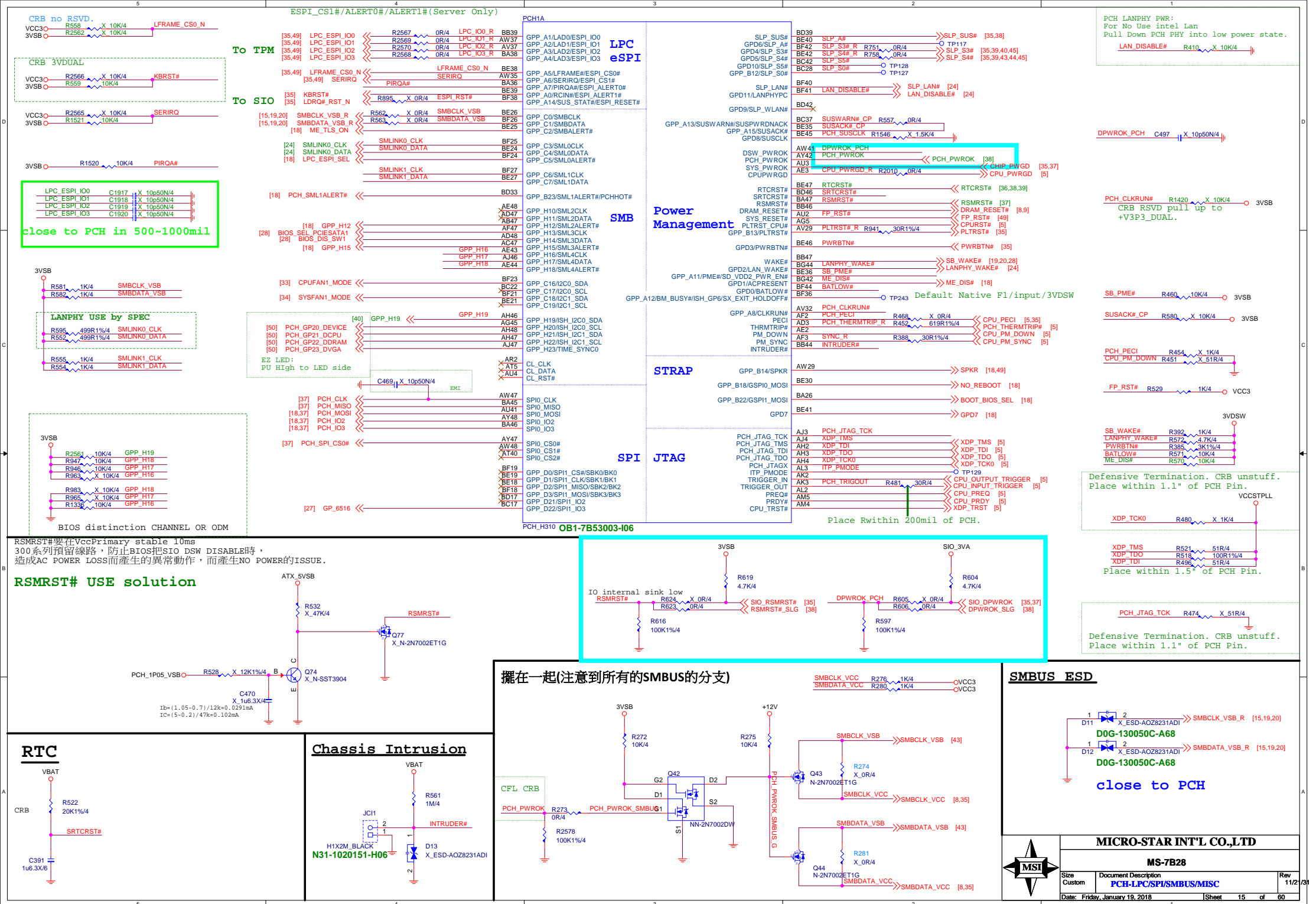
CNVi

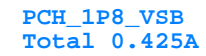
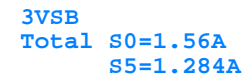
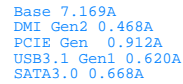
PCH_H310
OB1-7B53003-I06



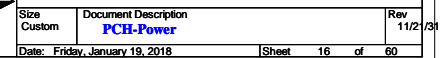
MS-7B28

Size Custom	Document Description PCH-GPIO/USBOC#/SATASTRAP	Rev 11/2/31
Date: Friday, January 19, 2018	Sheet 14 of 60	





內部只能推動這些POWER

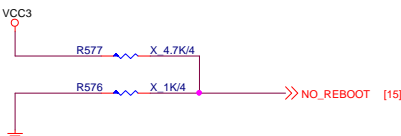


TOP Swap



Internal pull-down 20K is disabled after PLTRST#

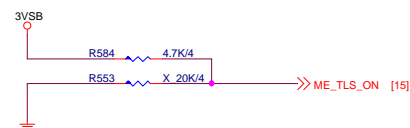
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

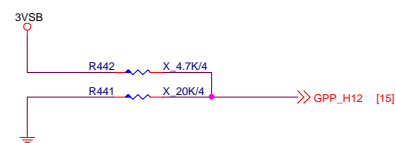
AMT and SBA with confidentiality



0 : DISABLE
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

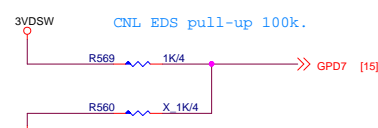
ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

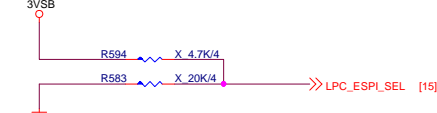
Internal pull-down 20K is disabled after RSMRST

Reserved



XTAL INPUT MODE
0 = XTAL INPUT IS SINGLE-ENDED
1 = XTAL INPUT IS DIFFERENTIAL
PCH HAS INTERNAL 20K PD

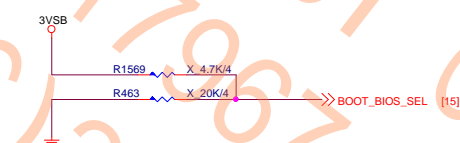
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

Boot BIOS

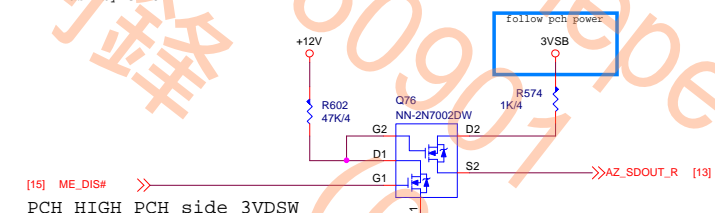


0 : SPI
1 : LPC

Internal pull-down 20K is disabled after PLTRST#

HDA_SDO

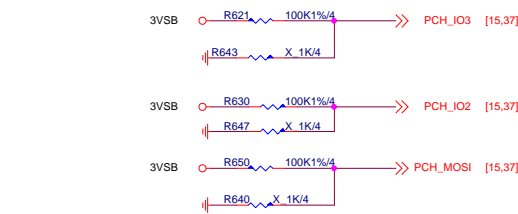
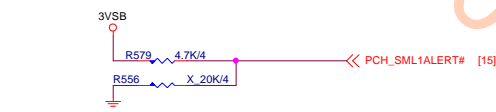
ME flash by GPIO



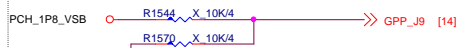
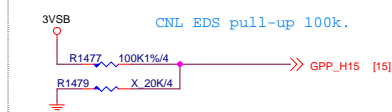
[15] ME_DIS#

PCH HIGH PCH side 3VDSW

Reserved

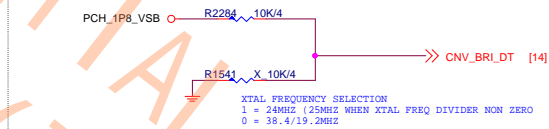


Reserved

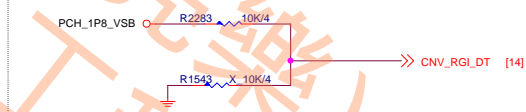


VCCSPI 3.3V, Internal pull-down.

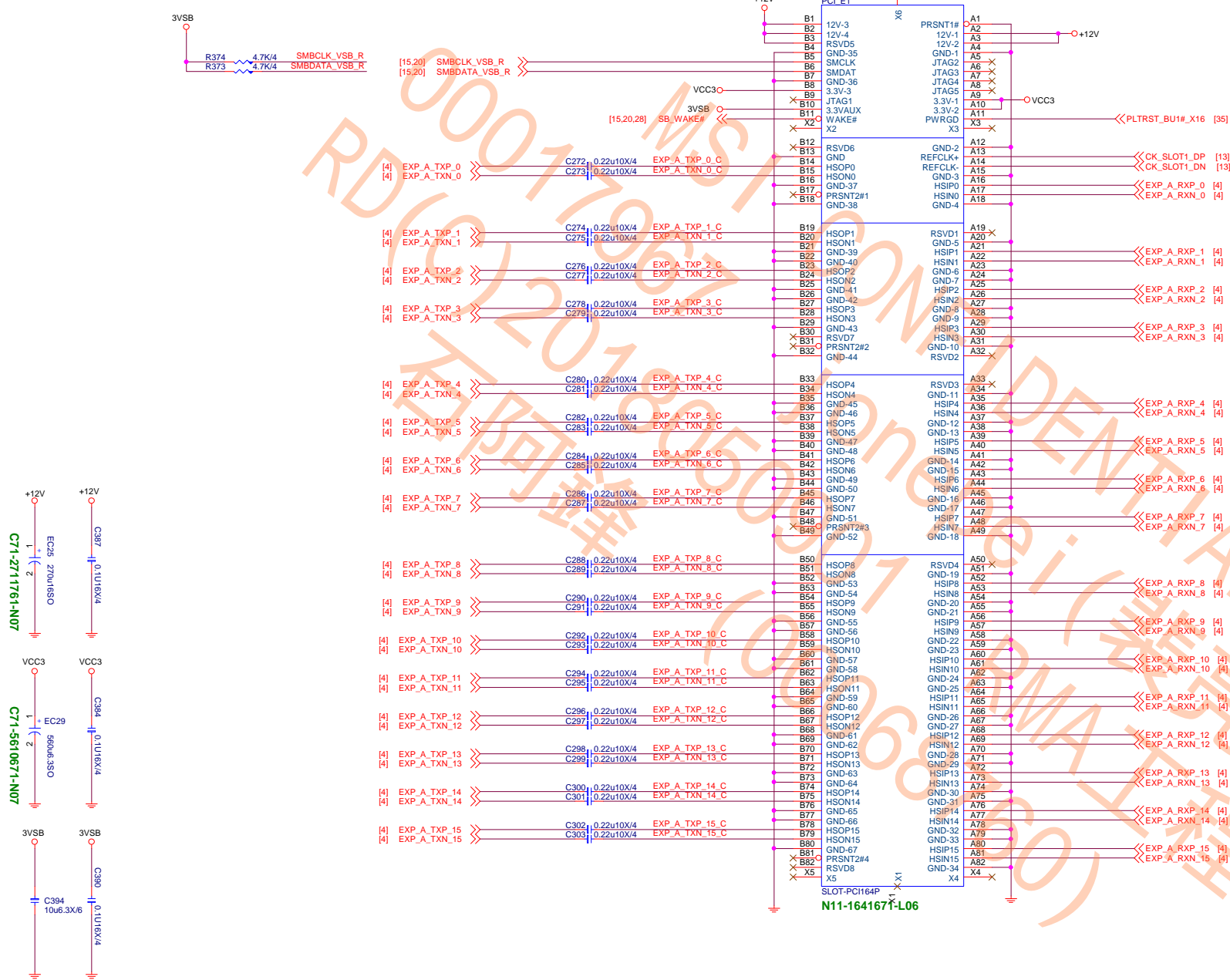
SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE
0 = VCCSPI IS CONNECTED TO 3.3V RAIL - DEFAULT
1 = VCCSPI IS CONNECTED TO 1.8V RAIL
PCH HAS INTERNAL 20K PD



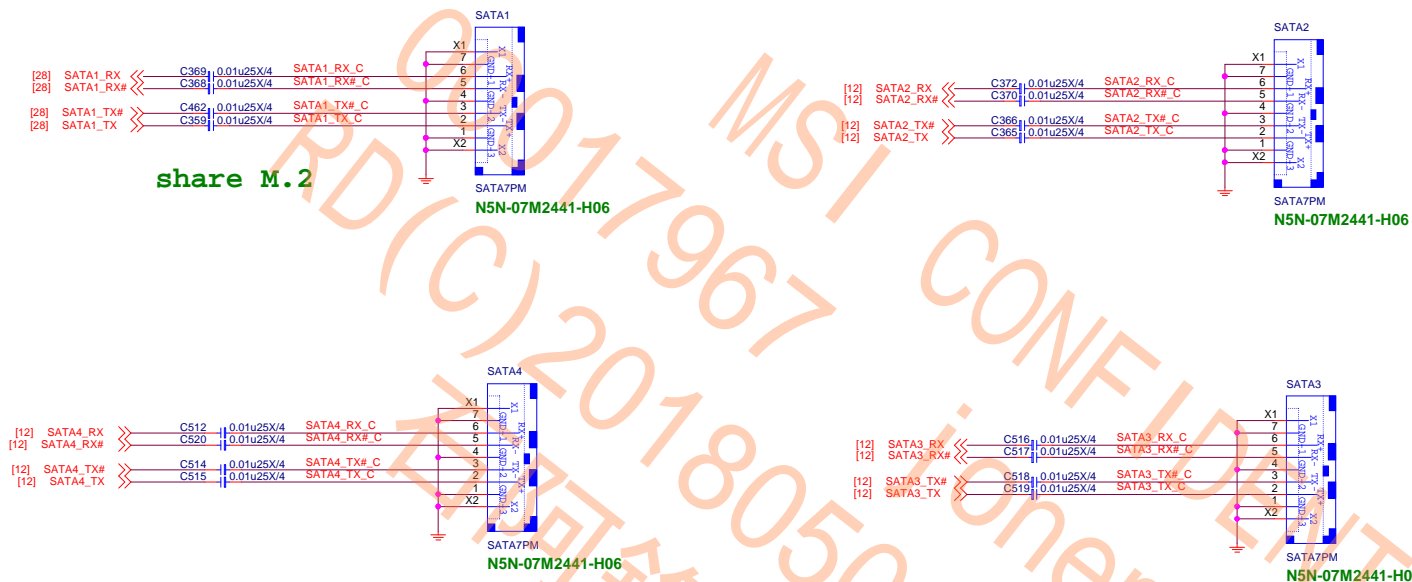
XTAL FREQUENCY SELECTION
1 = 24MHZ (25MHZ WHEN XTAL FREQ DIVIDER NON ZERO
0 = 38.4/19.2MHZ

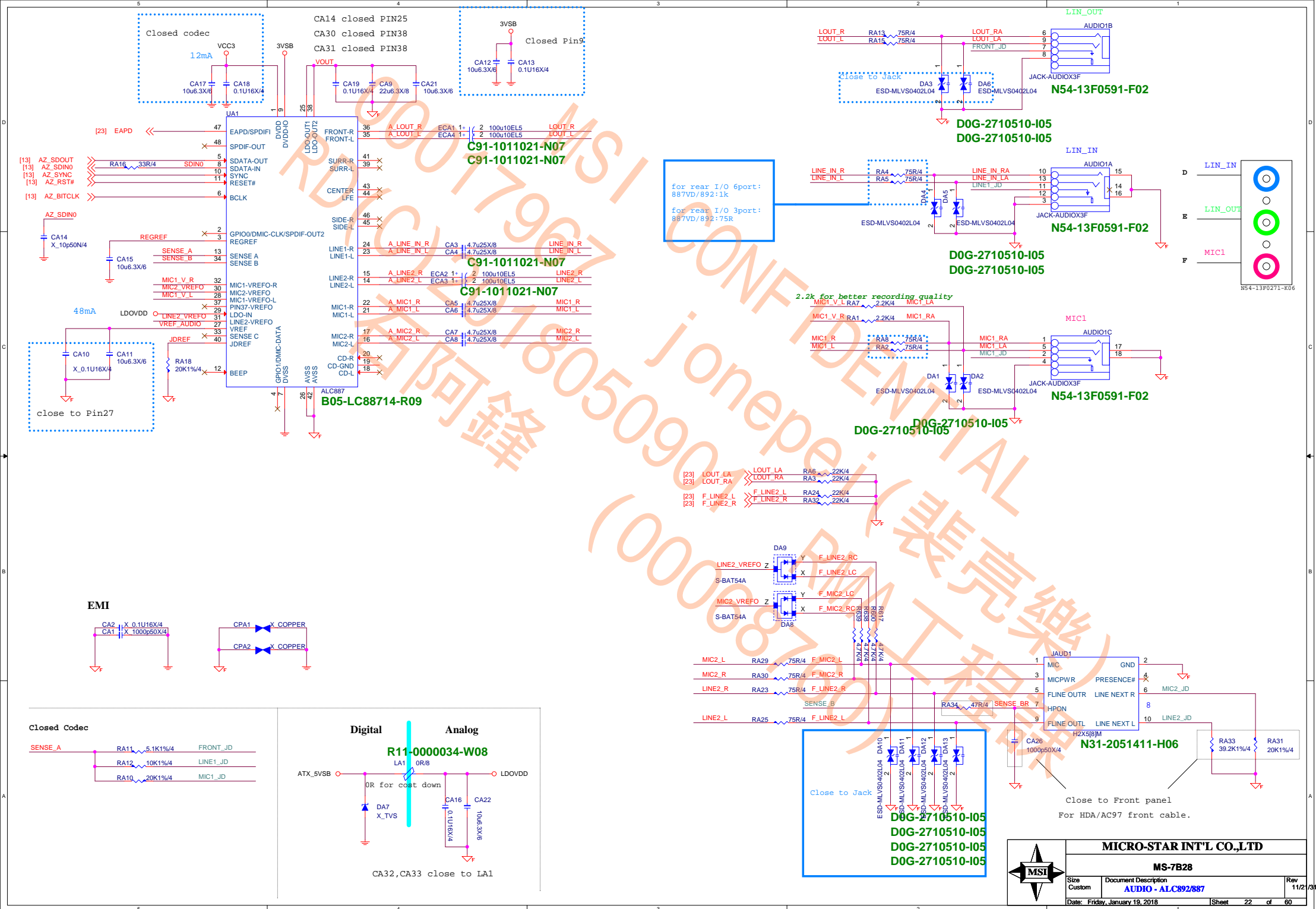


An external pull-up or pull-down is required.
0 = Integrated CNVi enable
1 = Integrated CNVi disable
Voltage level - 1.8V only



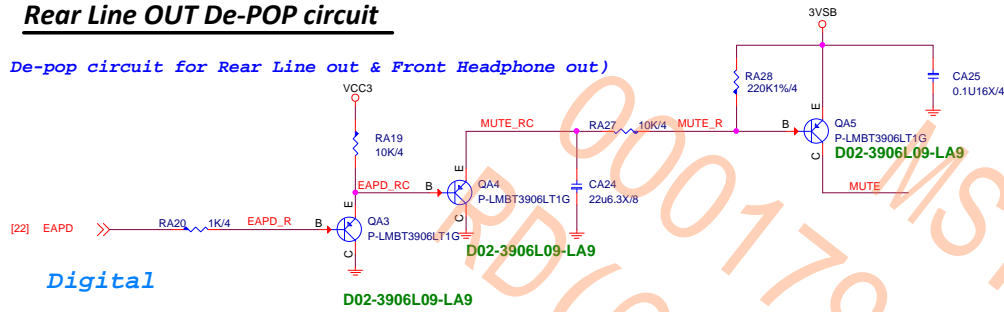
SATA 6G





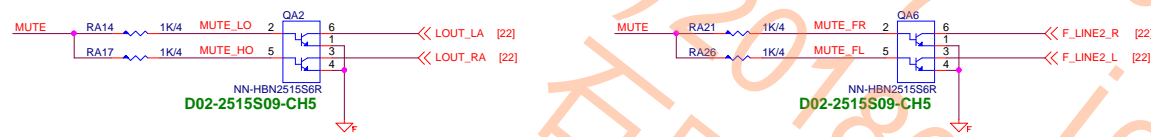
Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



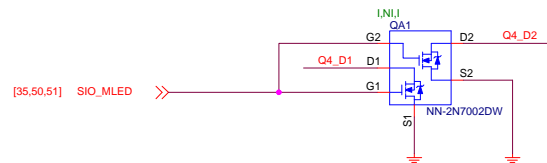
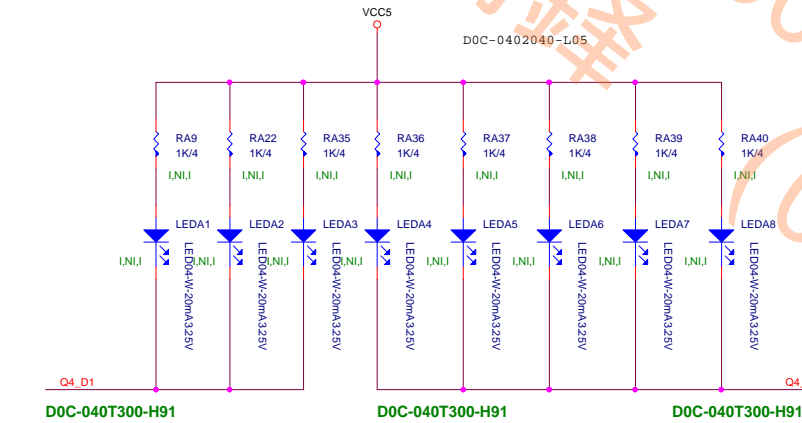
Digital

Analog



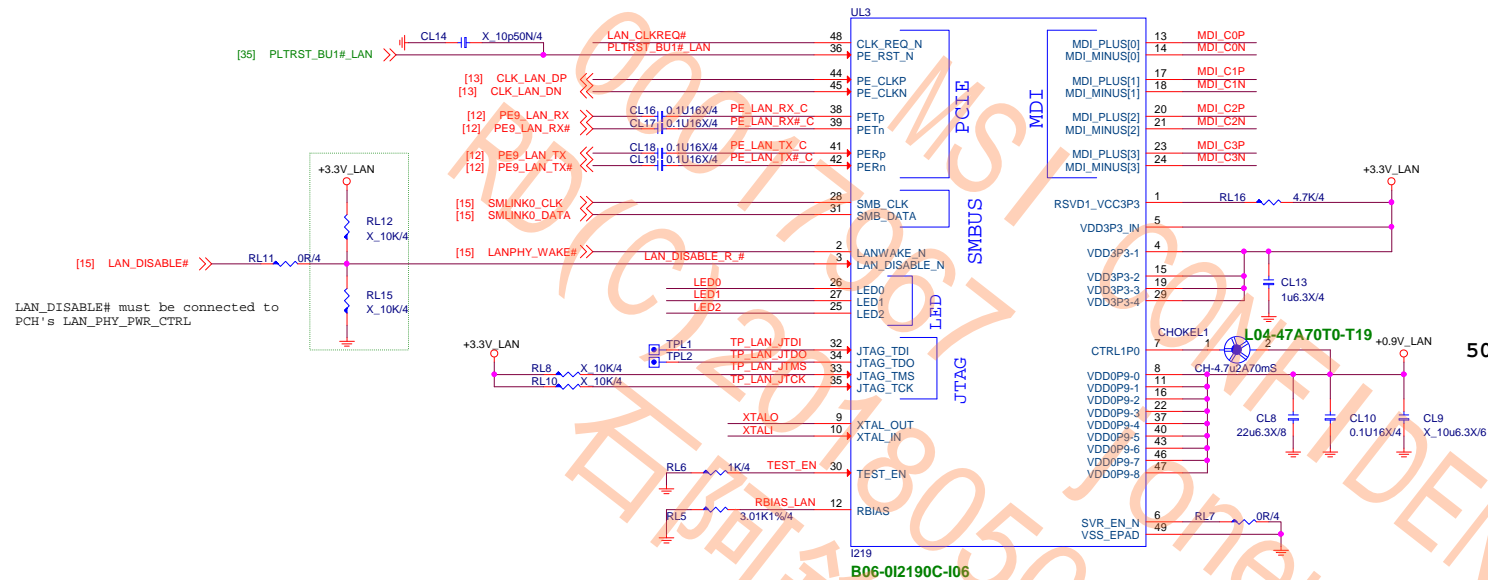
Audio moat is transparent and width 40mil

Audio LED

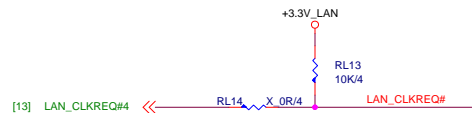


Schematic Cfg	Project
CFG1-7B38-H310 (H310M GAMING PLUS) ver.1.0	V A
CFG1-7B38-H310-APRO (H310-A Pro) ver.2.0	X B
CFG1-7B38-H310 (H310-A GAMING ARCTIC) ver.3.0	V C

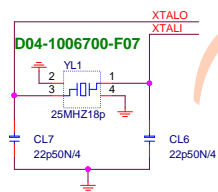
Intel Lan- I219



PCH's PCIECLKRQ<n> port mustbe mapped to PCH's PET/R<n+1>port.
If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN

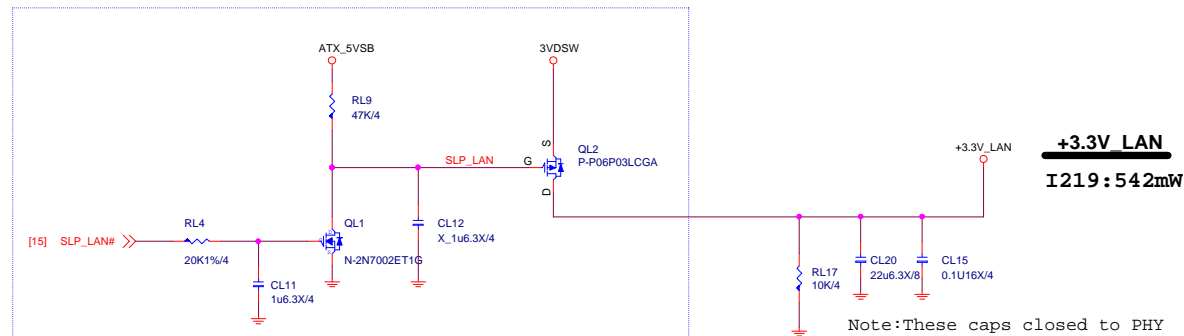


AVL:D04-1005700-SC6



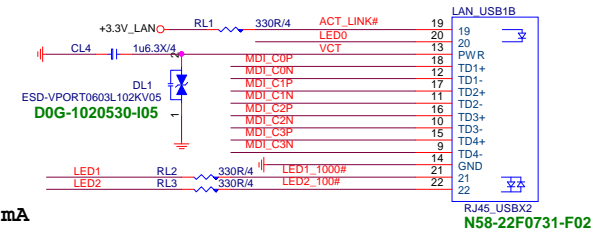
The 10Kohm pull-up resistor (RL18) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.

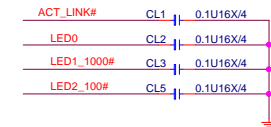


Note: These caps closed to PHY

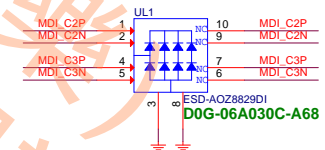
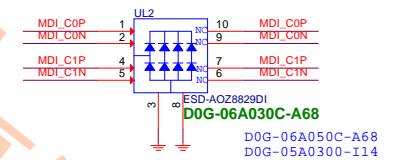
LAN Connector



For EMI



UL2&UL3 close to connector



Do not pair MDIO and MDI1 on the same TVSdevice (avoid LAN POE connecting issue). Otherpairing combination is ok.



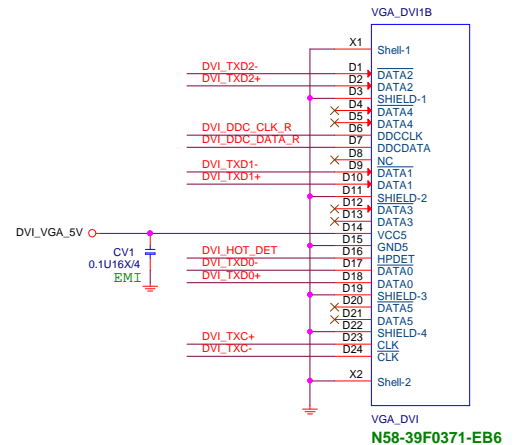
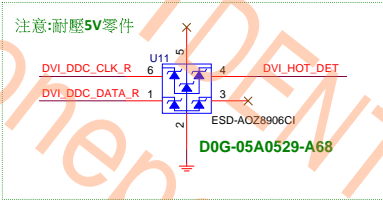
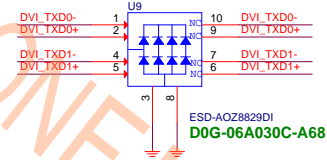
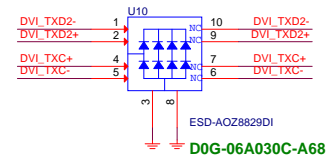
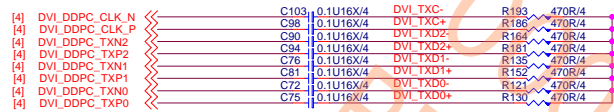
MICRO-STAR INT'L CO.,LTD

MS-7B28

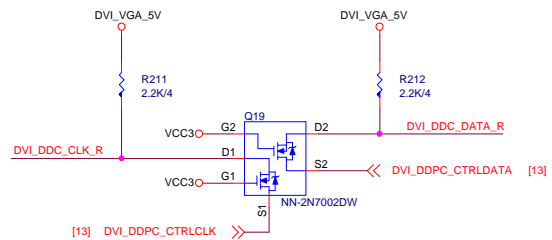
Size Custom	Document Description LAN - I219	Rev 11/21/3
Date: Friday, January 19, 2018		Sheet 24 of 60

DVI level shifter

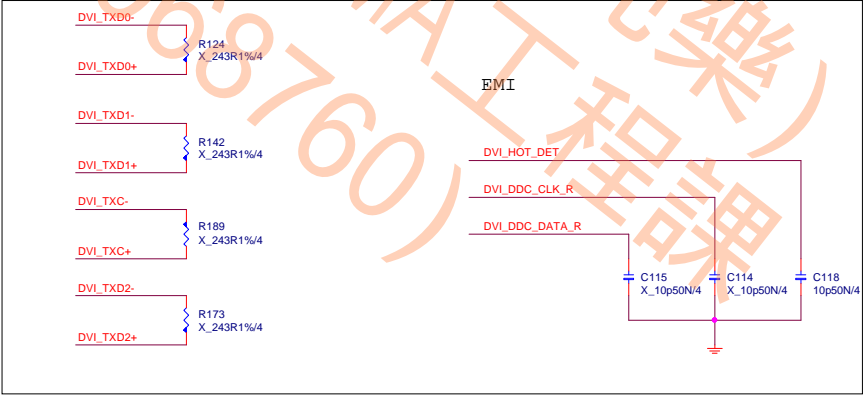
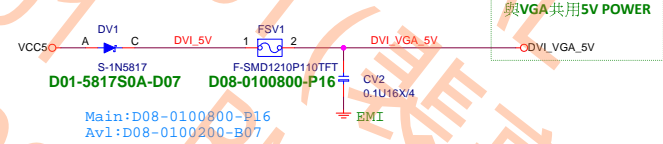
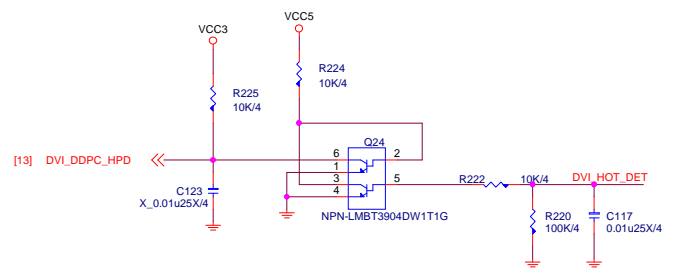
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



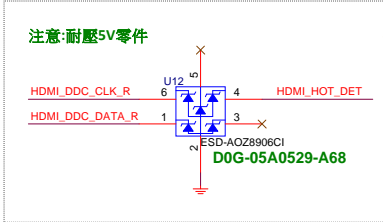
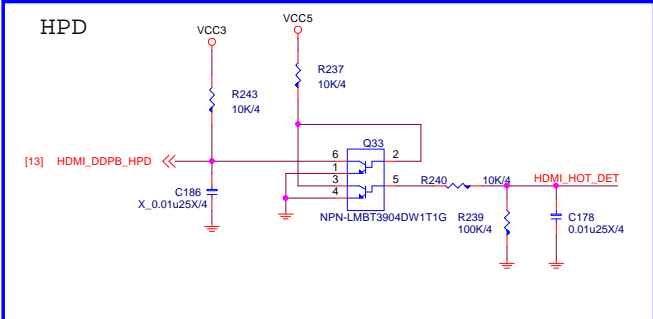
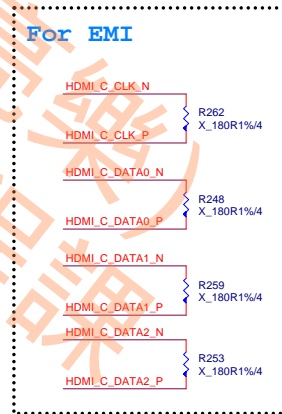
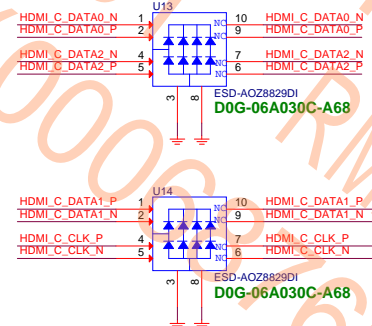
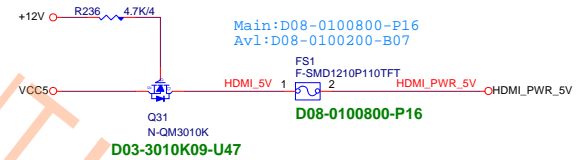
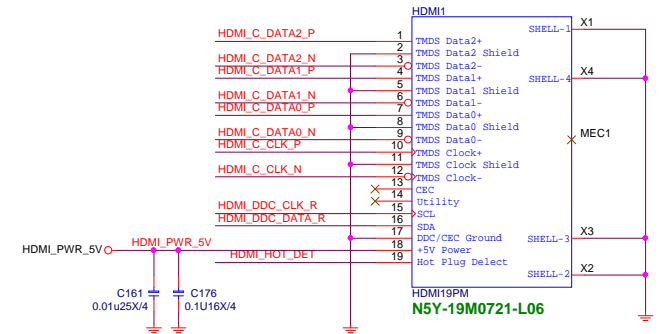
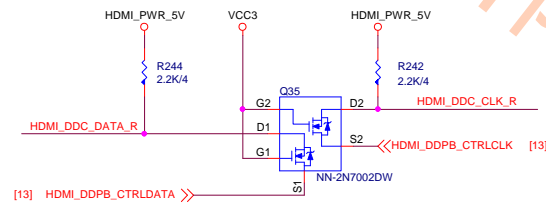
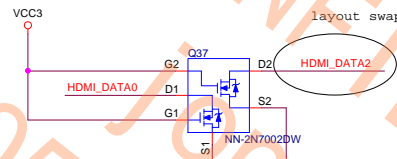
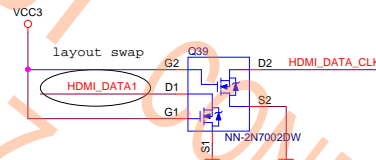
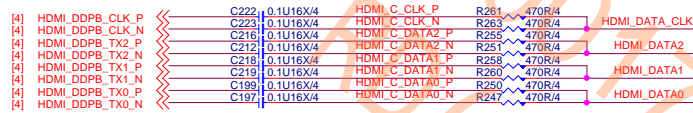
LEVEL SHIFT using I2C Repeater



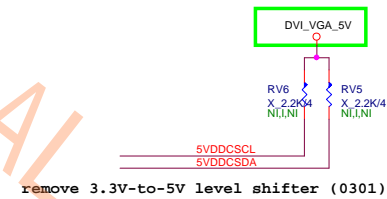
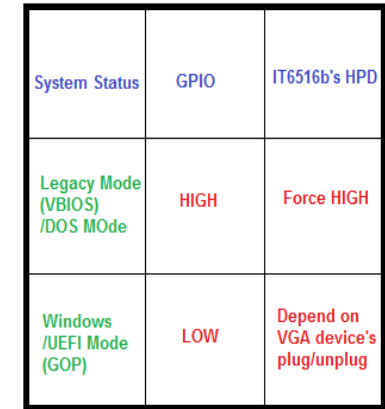
HPD



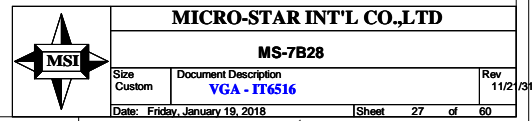
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

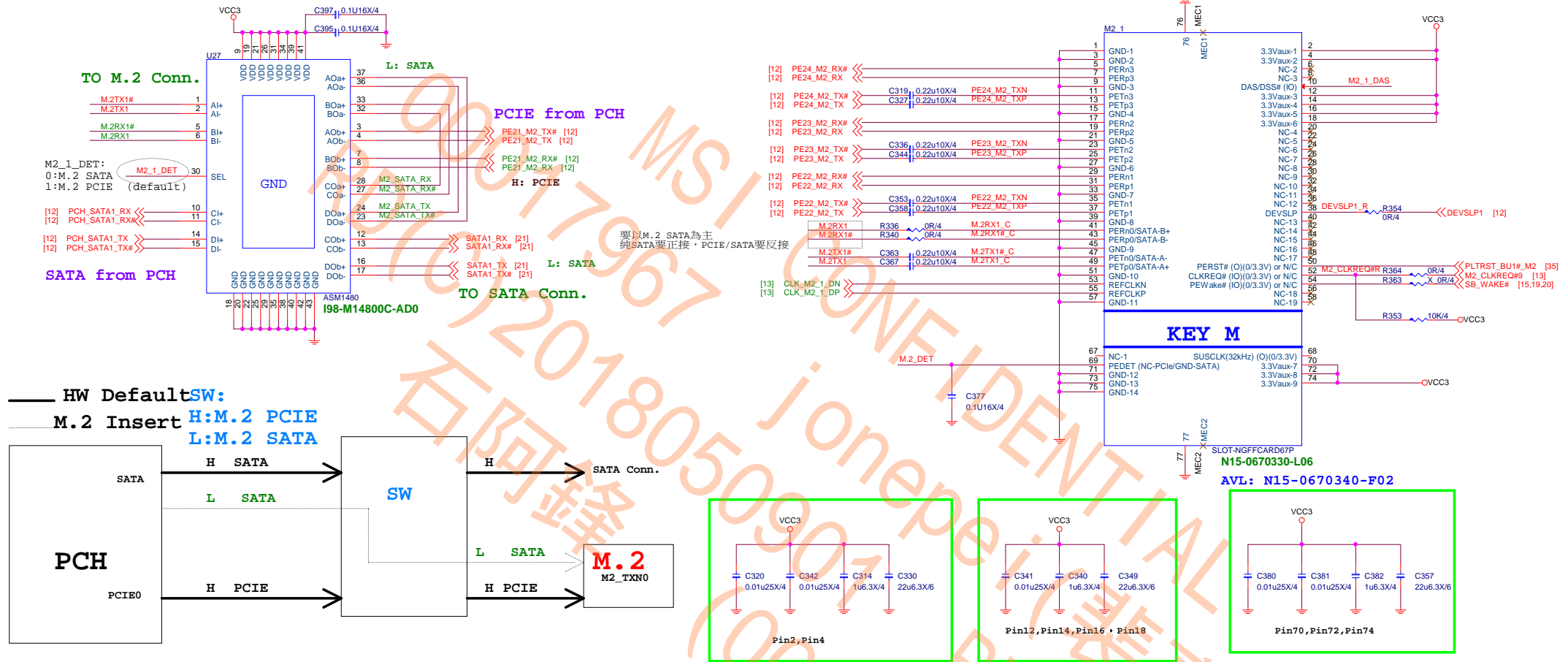


If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

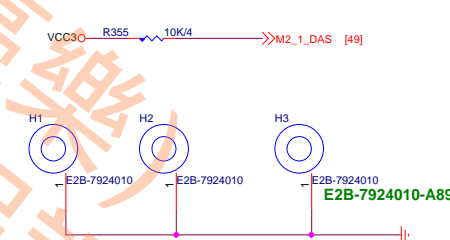
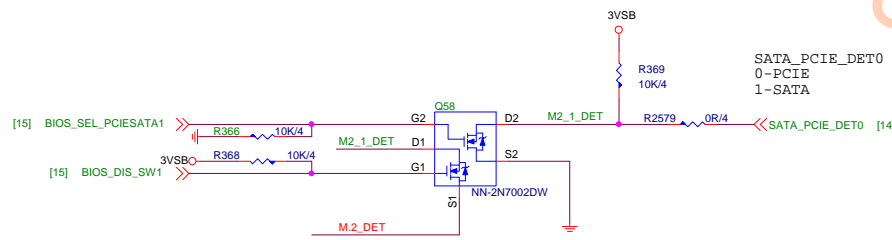
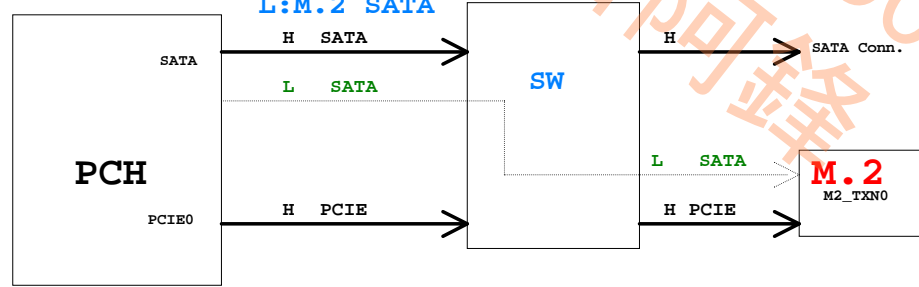


Schematic Cfg	Project	
CFG1-7B38-H310 (H310M Gaming)	X	A
CFG1-7B38-H310-APRO (H310-A Pro)	V	B

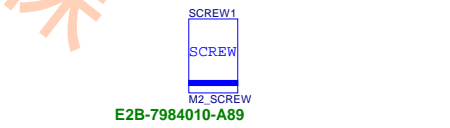




HW Default SW:
M.2 Insert H:M.2 PCIE
L:M.2 SATA



BIOS_DIS_SW1	BIOS_SEL_PCIESATA1	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI	GPI	AUTO



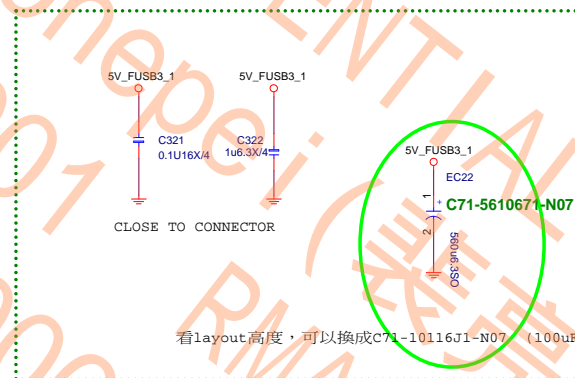
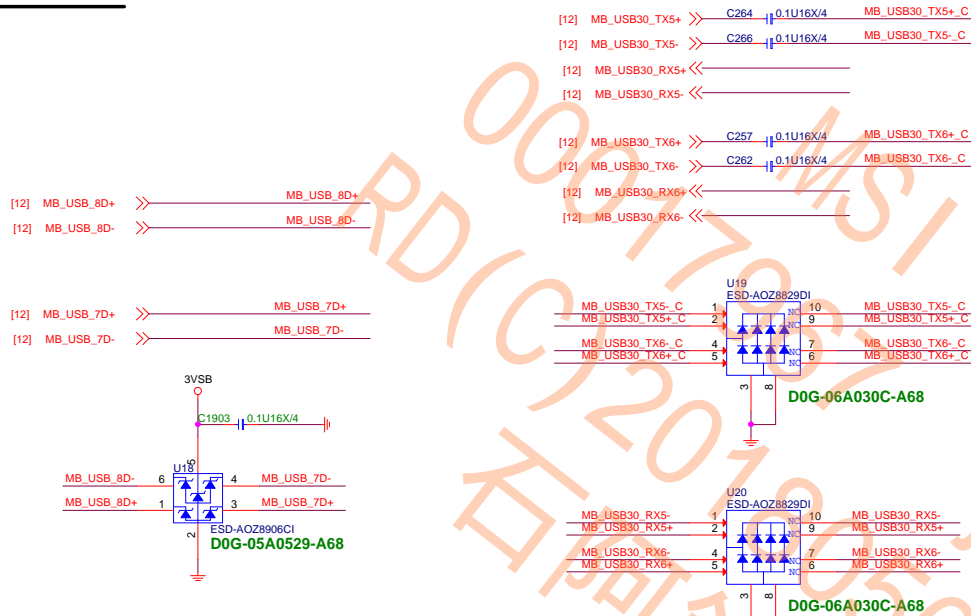
MICRO-STAR INT'L CO.,LTD

MS-7B28

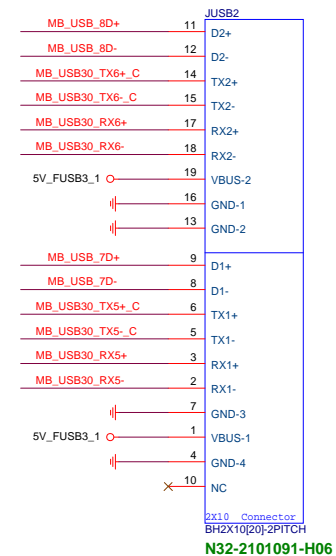
Size Custom Document Description **M2-SLOT1** Rev 11/2/31

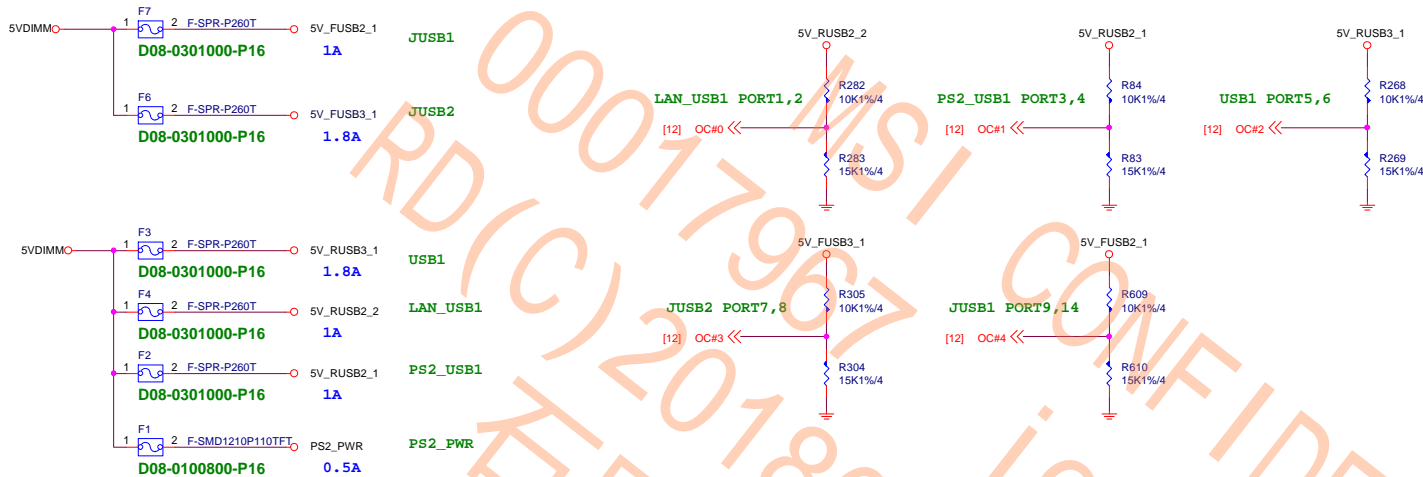
Date: Friday, January 19, 2018 Sheet 28 of 60

Front JUSB3 port 7,8



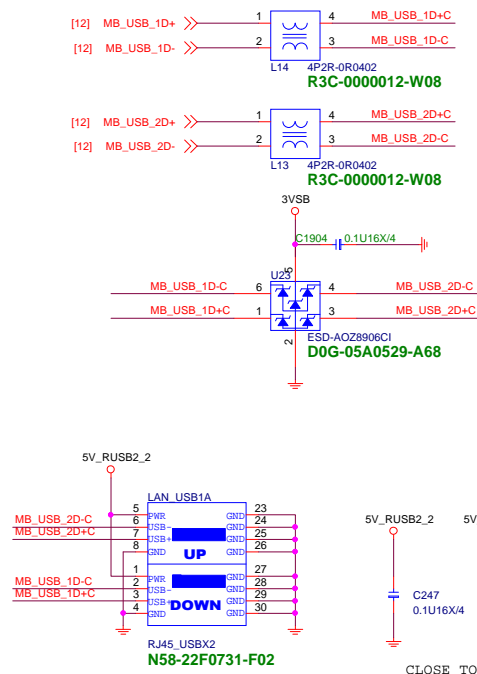
看layout高度，可以換成C71-10116J1-N07 (100uF)



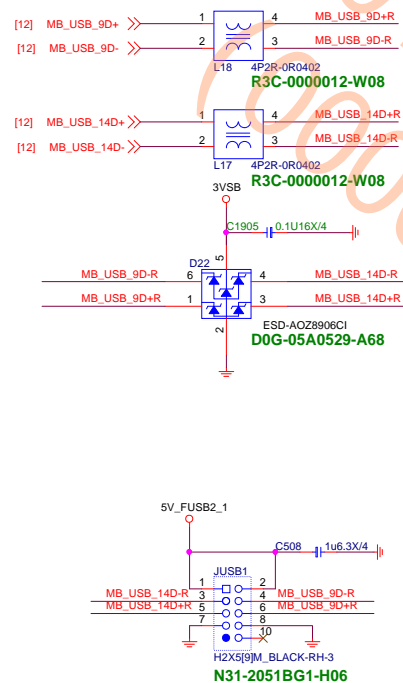


USB CONN	USB POWER	PCH PORT	OC# SIGNAL
LAN_USB1	5V_RUSB2_2	Port1,2	OC#0
PS2_USB1	5V_RUSB2_1	Port3,4	OC#1
USB1	5V_RUSB3_1	Port5,6	OC#2
JUSB2	5V_FUSB3_1	Port7,8	OC#3
JUSB1	5V_FUSB2_1	Port9,14	OC#4

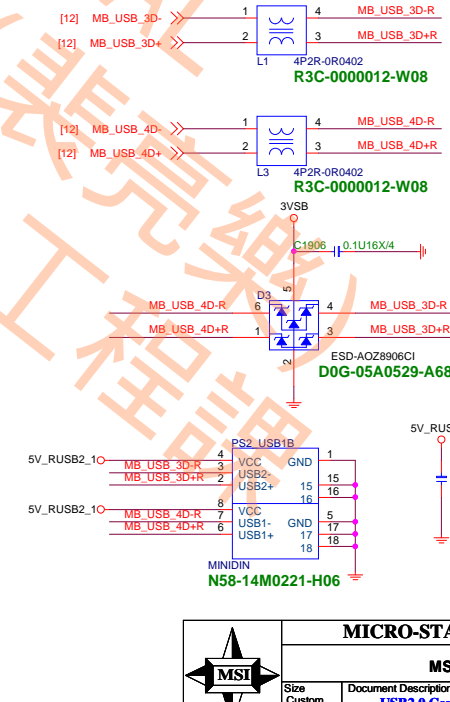
Rear USB1 port 1,2



JUSB1 PORT 9,14

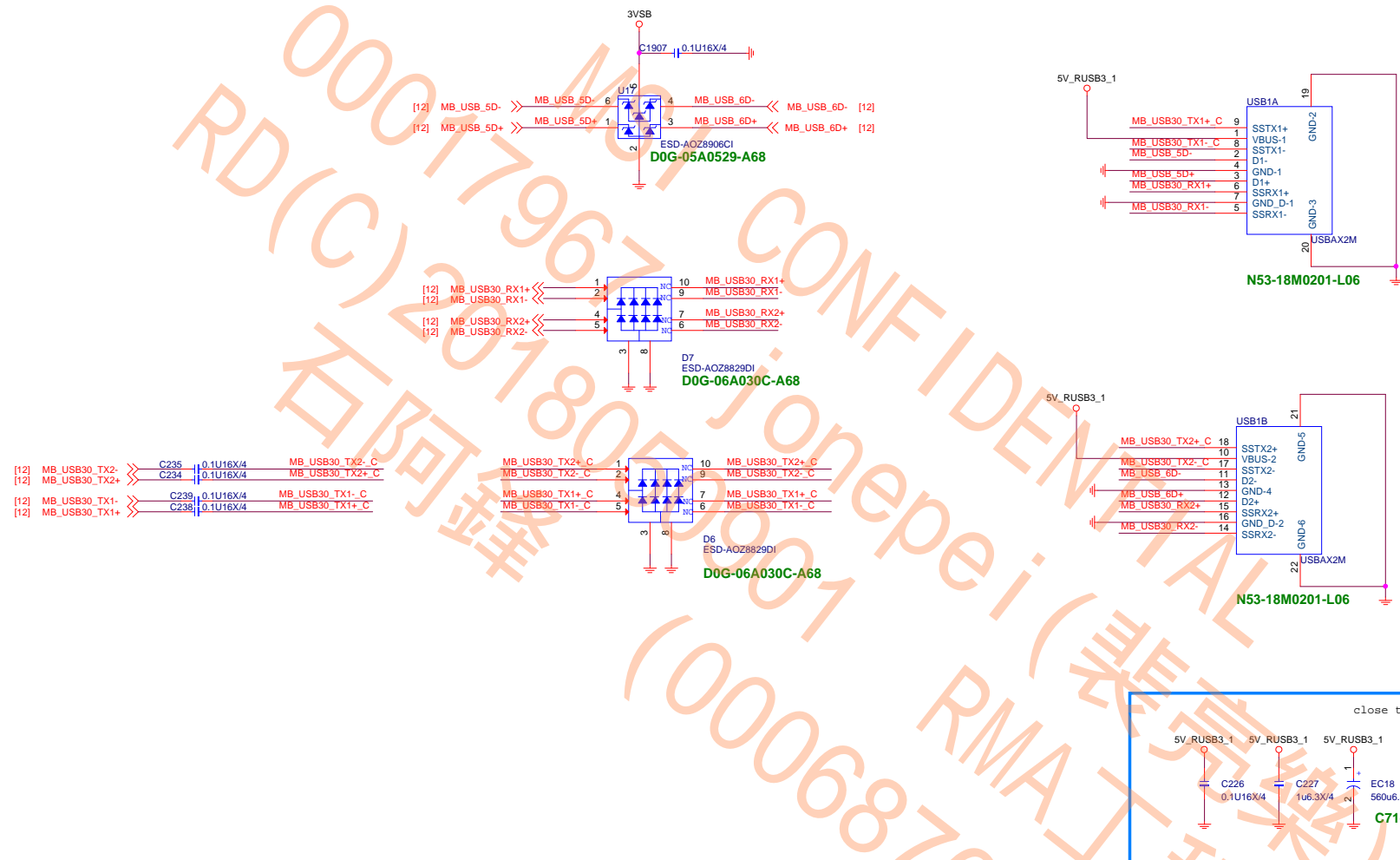


PS2_USB1 PORT 3,4



MICRO-STAR INT'L CO.,LTD			
MS-7B28			
Size	Document Description	Rev	
Custom	USB2.0 Connector	11/2	
Date: Friday, January 19, 2018		Sheet	30 of 60

REAR USB1 Connect

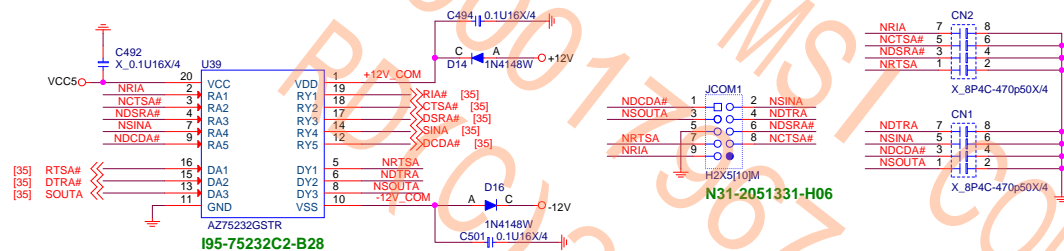


MICRO-STAR INT'L CO.,LTD

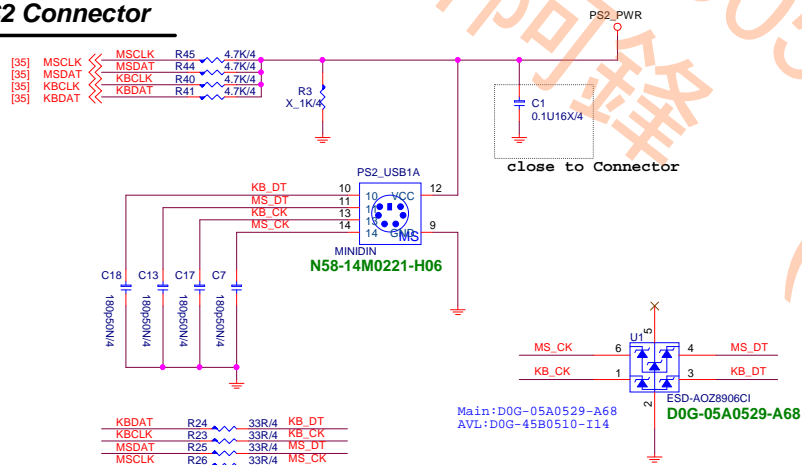
MS-7B28

Size Custom	Document Description REAR USB1 Connect	Rev 11/21/3
Date: Friday, January 19, 2018		Sheet 31 of 60

SERIAL PORT 1



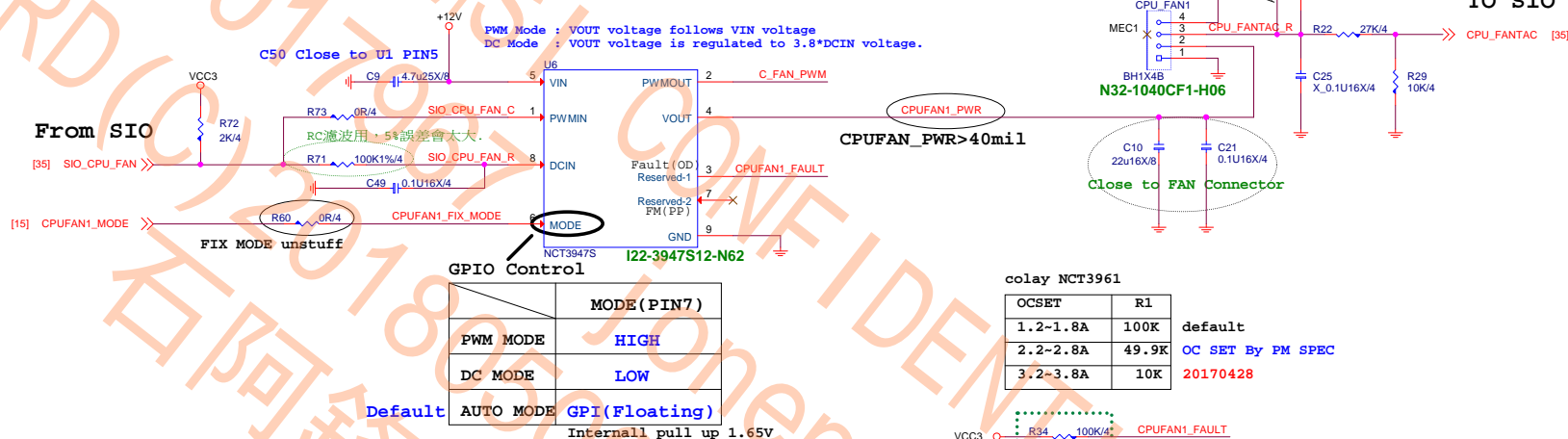
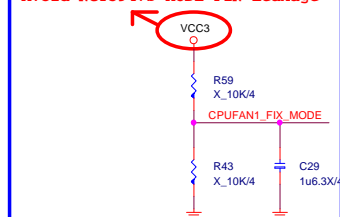
PS2 Connector



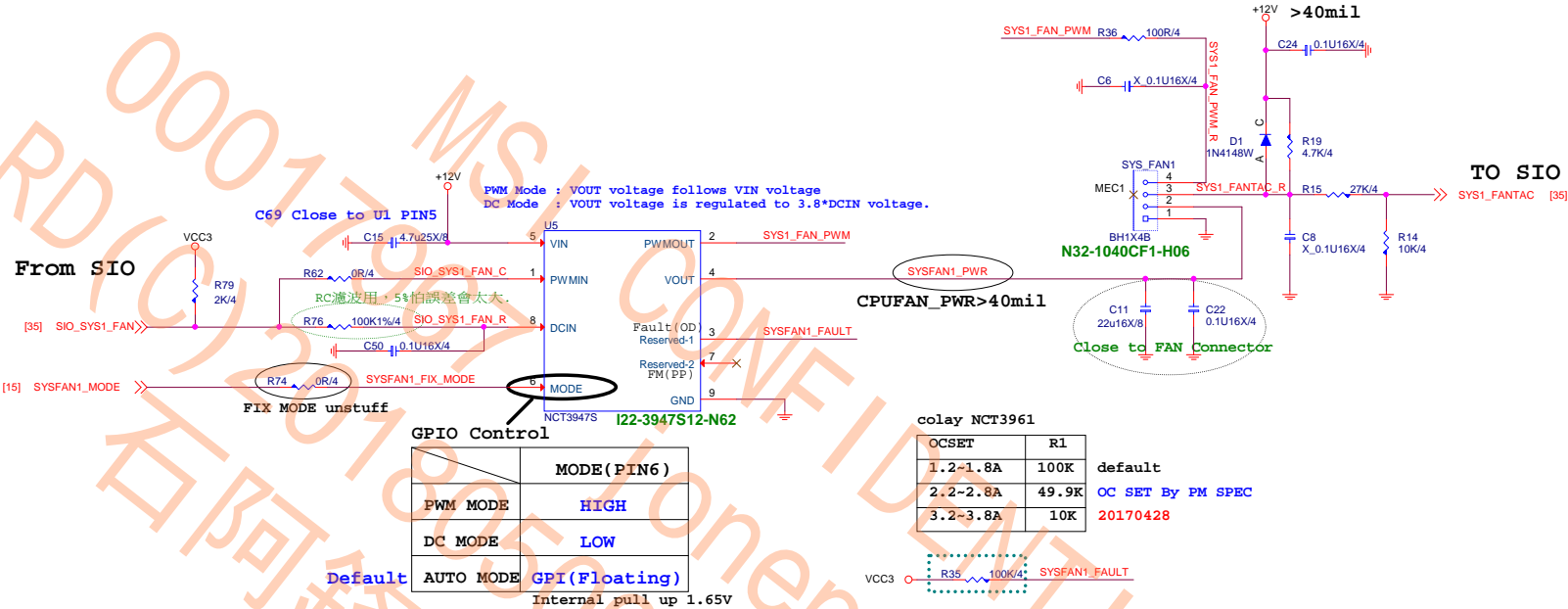
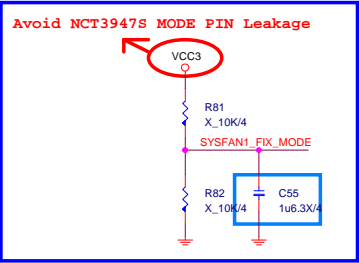
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

GPIO可以由BIOS切换 PWM/DC MODE

Avoid NCT3947S MODE PIN Leakage



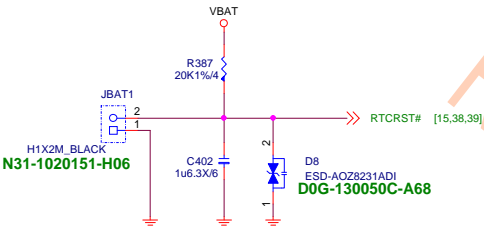
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



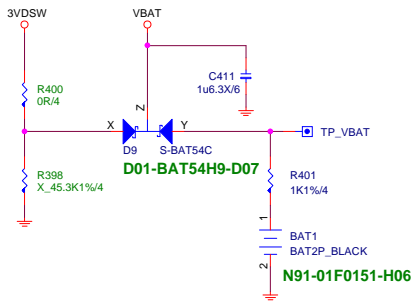
GPIO Control	
	MODE(PIN6)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)
Internal pull up 1.65v	

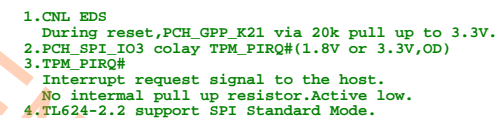
colay NCT3961	
OCSET	R1
1.2~1.8A	100K
2.2~2.8A	49.9K
3.2~3.8A	10K
default	
OC SET By PM SPEC	
20170428	

Cut VBAT

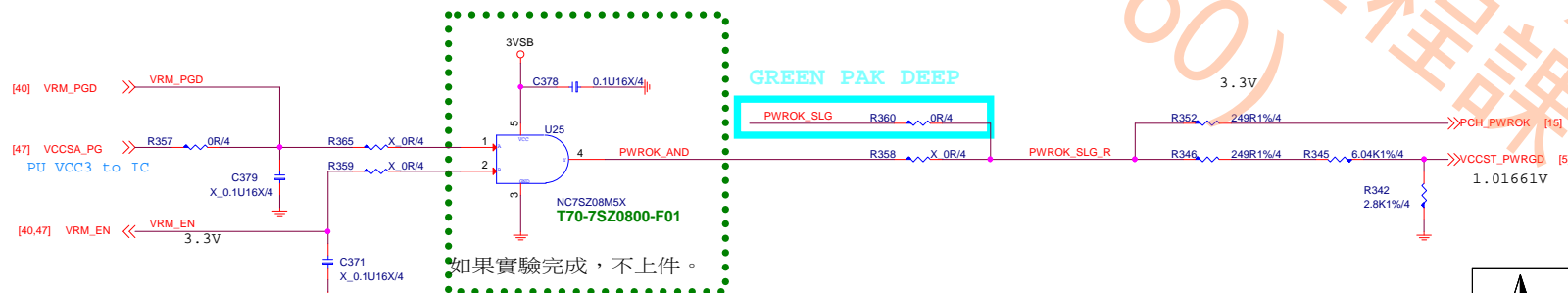
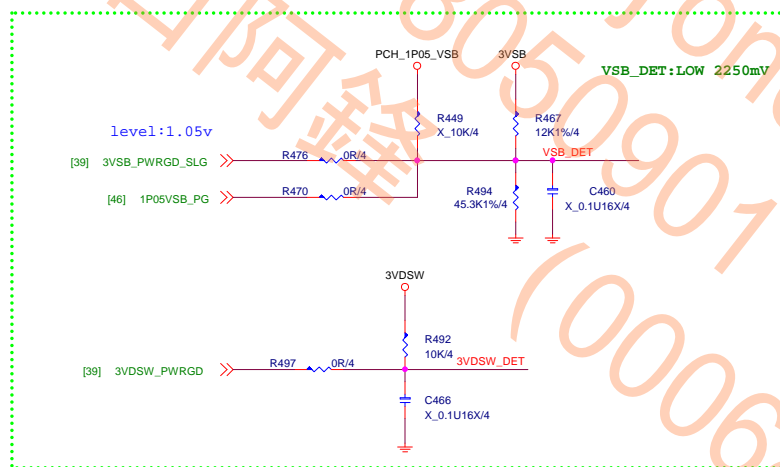
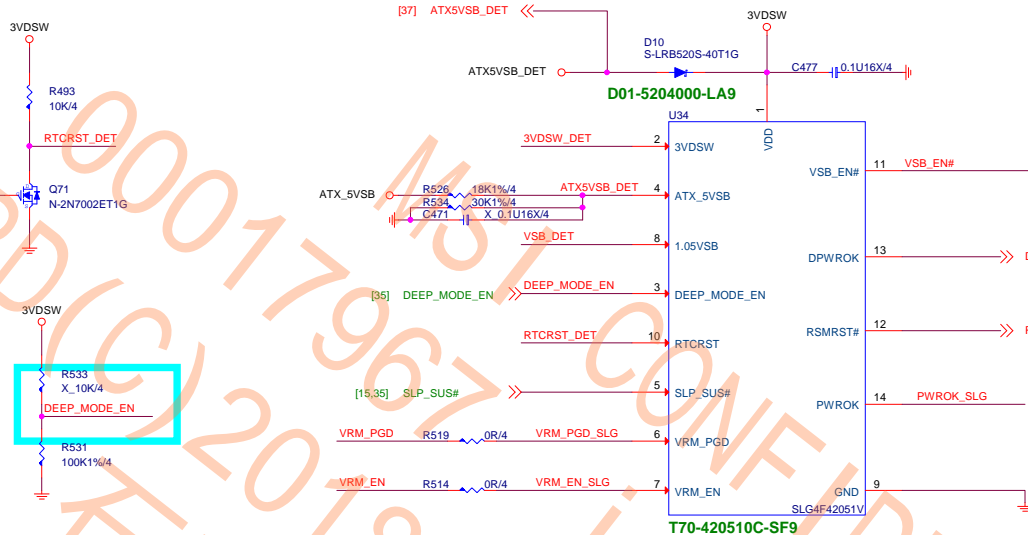


VBAT





	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0

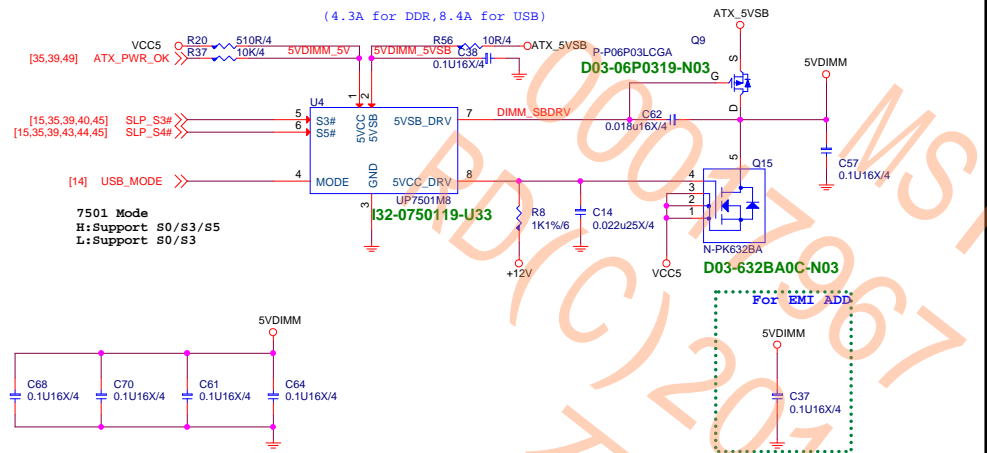


如果實驗完成，不上件。

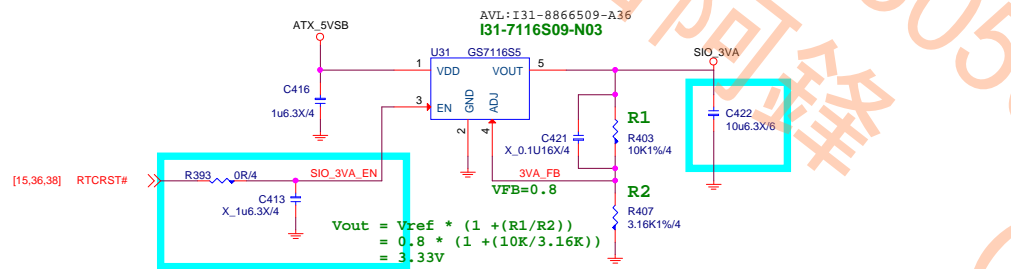


MICRO-STAR INT'L CO.,LTD		
MS-7B28		
Size	Document Description	Rev
Custom	GREEN PAK DEEP	11/2
Date: Friday, January 19, 2018	Sheet 38 of 60	

5VDIMM@5V/11.3075A

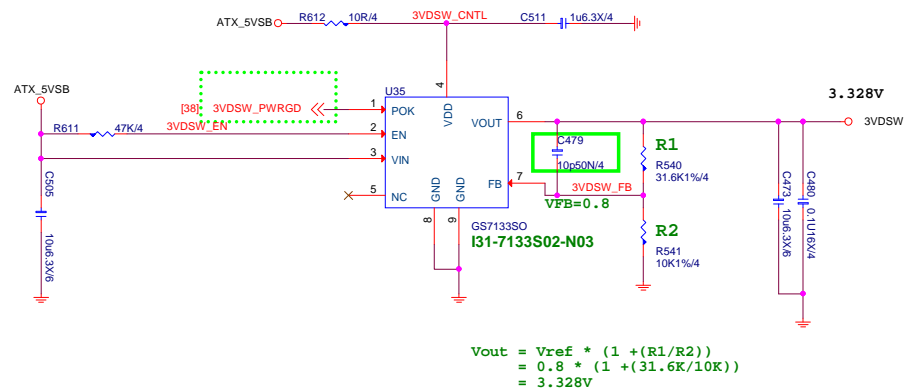


SIO_3VA@3.3V/20mA



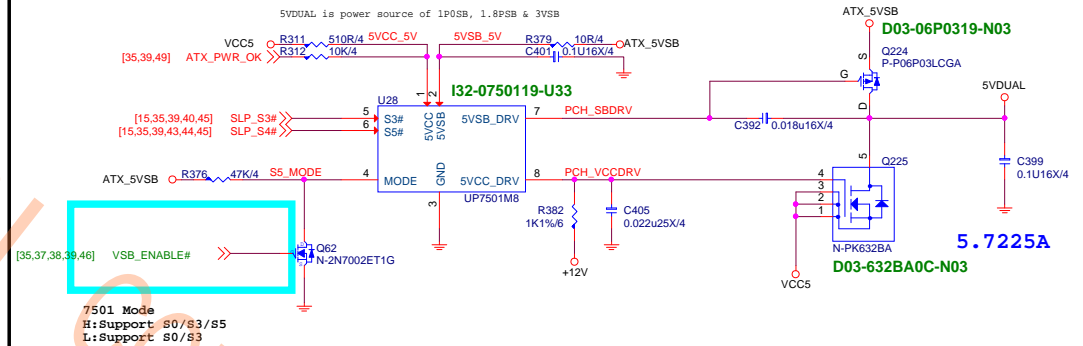
3VDSW@3.3V/0.3A

Intel Lan 不能用小顆IC，因為LAN瞬間電流會很大。
113mA(PCH)+0.6mA(RTC)+200mA(LAN-I219)+SIO



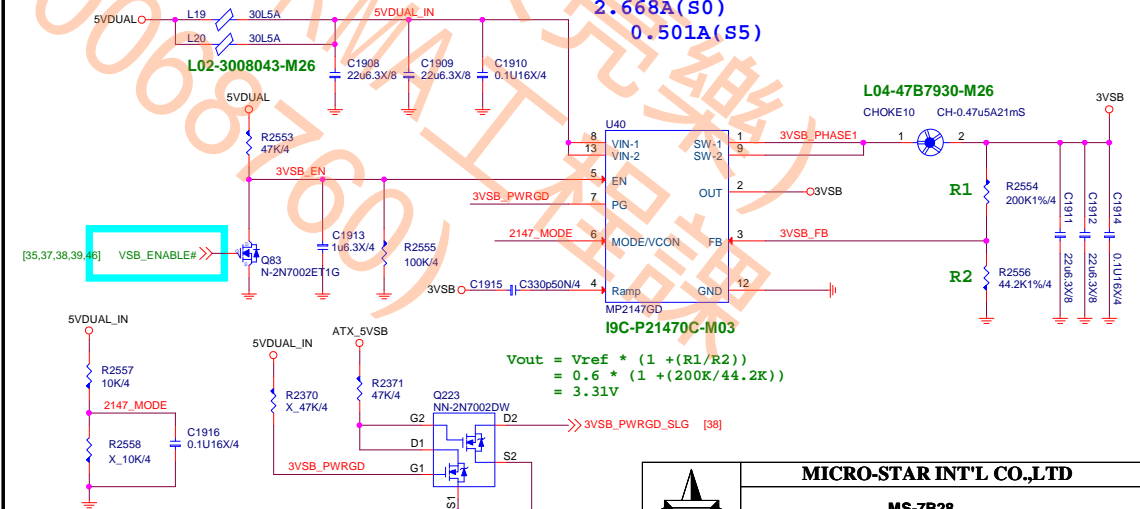
5VDUAL@5V/5.7225A

5VDUAL is power source of 1P0SB, 1.8PSB & 3VSB

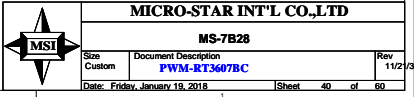


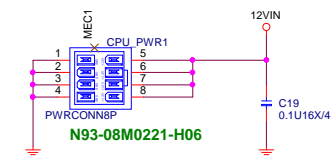
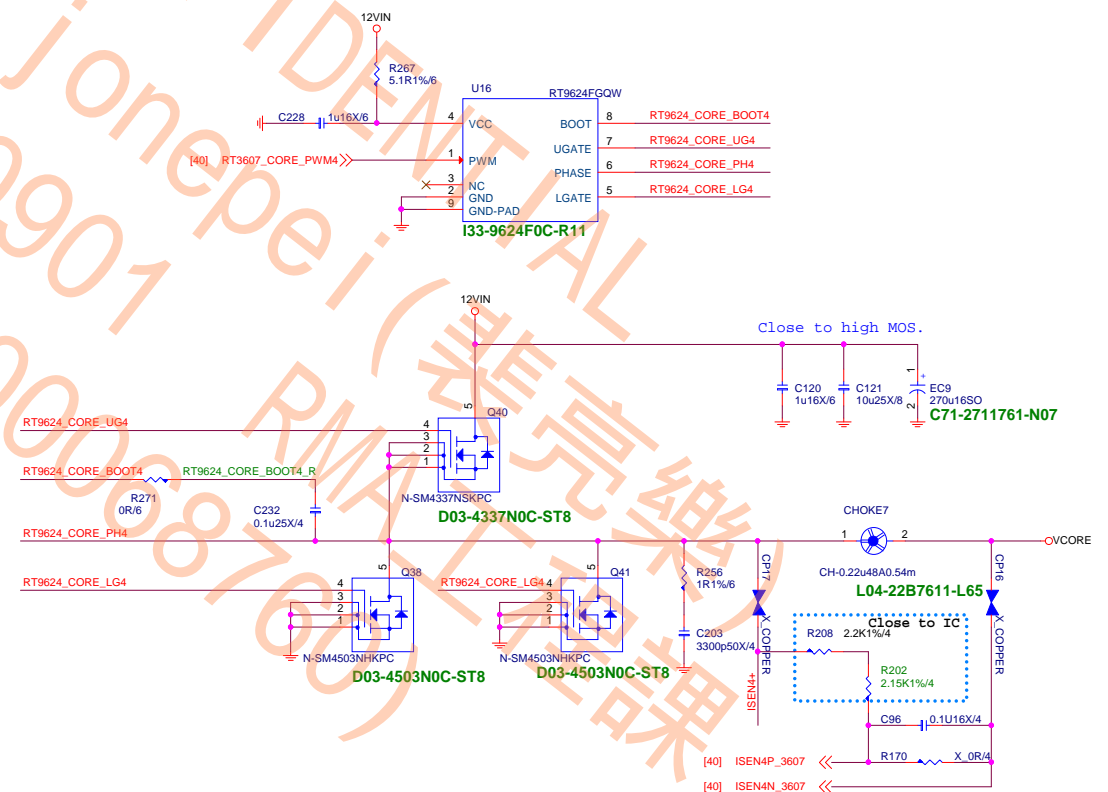
3VSB cost down@3.3V/3.281A 2.253A(PCH)+0.415A(PE SLOT*3)

2.668A(S0)
0.501A(S5)



MICRO-STAR INT'L CO.,LTD		
MS-7B28		
Size Custom	Document Description ACPI CONTROLLER	Rev 11/2
Date: Friday, January 19, 2018	Sheet 39 of 60	



[illegible]

MS-7B28

Size Custom	Document Description VCORE(P-PAK) PHASE1-4	Rev 11/21/3
Date: Friday, January 19, 2018		Sheet 41 of 60

VCC_DDR@1.2V/11.525A

$$DDR4_1.2V\ 3.3A+7.85A+0.375A=11.525A$$

3.3A FOR CPU
10A FOR 2DIMM DDR4
0.375A FOR VTT_DDR

$$Rlimit = Llimit * Rds * 10 / 5uA$$

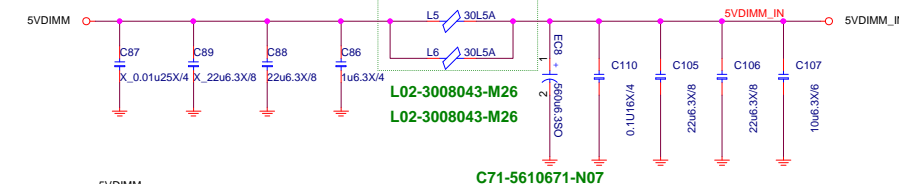
$$Rlimit = 14.9825 * 4 / 10 / 5$$

D03-632BA0C-N03
Current limit= 118K*5uA/10/4mohm=14.75A

$$0.4V < Rlimit * 5uA < 3V$$

VID	Reference Voltage (V)
H	0.675
L	0.75

Input Current= (11.525A*1.2V)/5V/0.8=3.4575A
L02-3008043-M26
Over 85°C ,Rated Current 1.5A.



$$I_{rms} = I_{out} * \sqrt{((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))}$$

$$= 11.525 * \sqrt{0.427}$$

$$= 4.921175A$$

$$DDR\ OCP = R44 * 5uA / 10 / Dds(on)$$

$$138k * 5uA / 10 / 3m = 23A$$

$$138k * 5uA / 10 / 4.6m = 15A$$

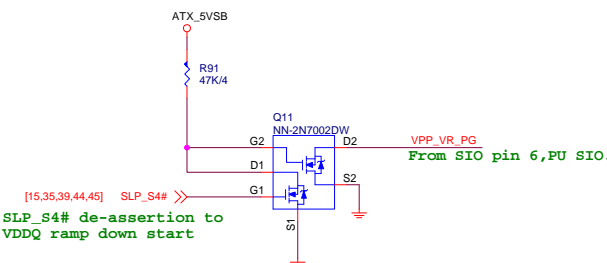
MOS Rds(on) 是 3m~4.6m ohm

VTT 固定2.6A
Current Limit 2.6A

$$V_{out} = V_{ref} * (1 + (R1/R2))$$

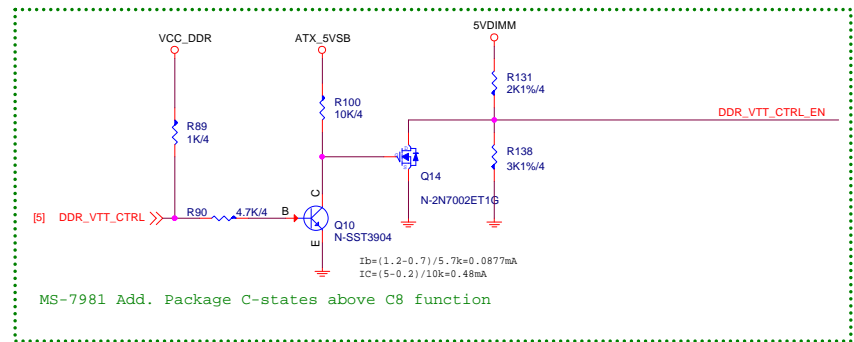
$$= 0.75 * (1 + (1K/1.65K))$$

$$= 1.204V$$



SLP_S4# de-assertion to VDDQ ramp down start

VPP ramp down after VDDQ ramp down



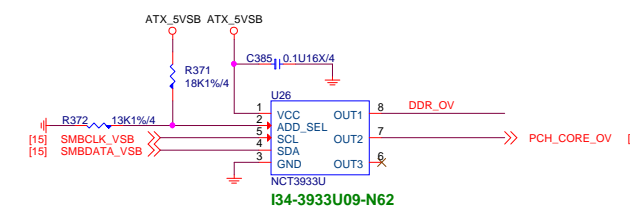
$$I_b = (1.2 - 0.7) / 5.7k = 0.0877mA$$

$$I_c = (5 - 0.2) / 10k = 0.48mA$$

MS-7981 Add. Package C-states above C8 function

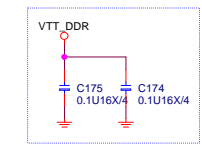
UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



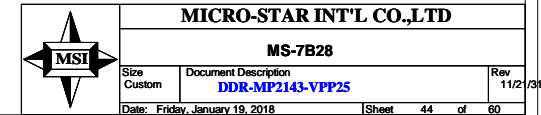
MAX:11.525A
1.2V

0.1uFx1 per dimm

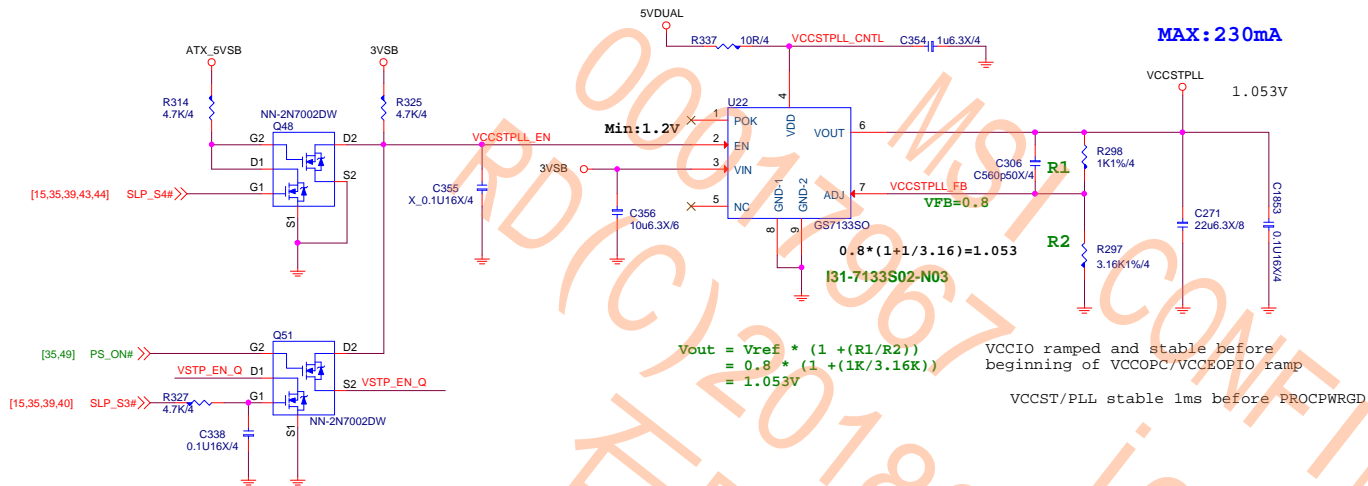


MICRO-STAR INT'L CO.,LTD		
MS-7B28		
Size	Document Description	Rev
Custom	DDR-RT8231	11/2
Date: Friday, January 19, 2018	Sheet 43 of 60	

DDR VPP 固定4.8A

$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.6 * (1 + (196K/61.9K)) \\ &= 2.4998V \end{aligned}$$


VCCSTPLL@1.05V/230mA

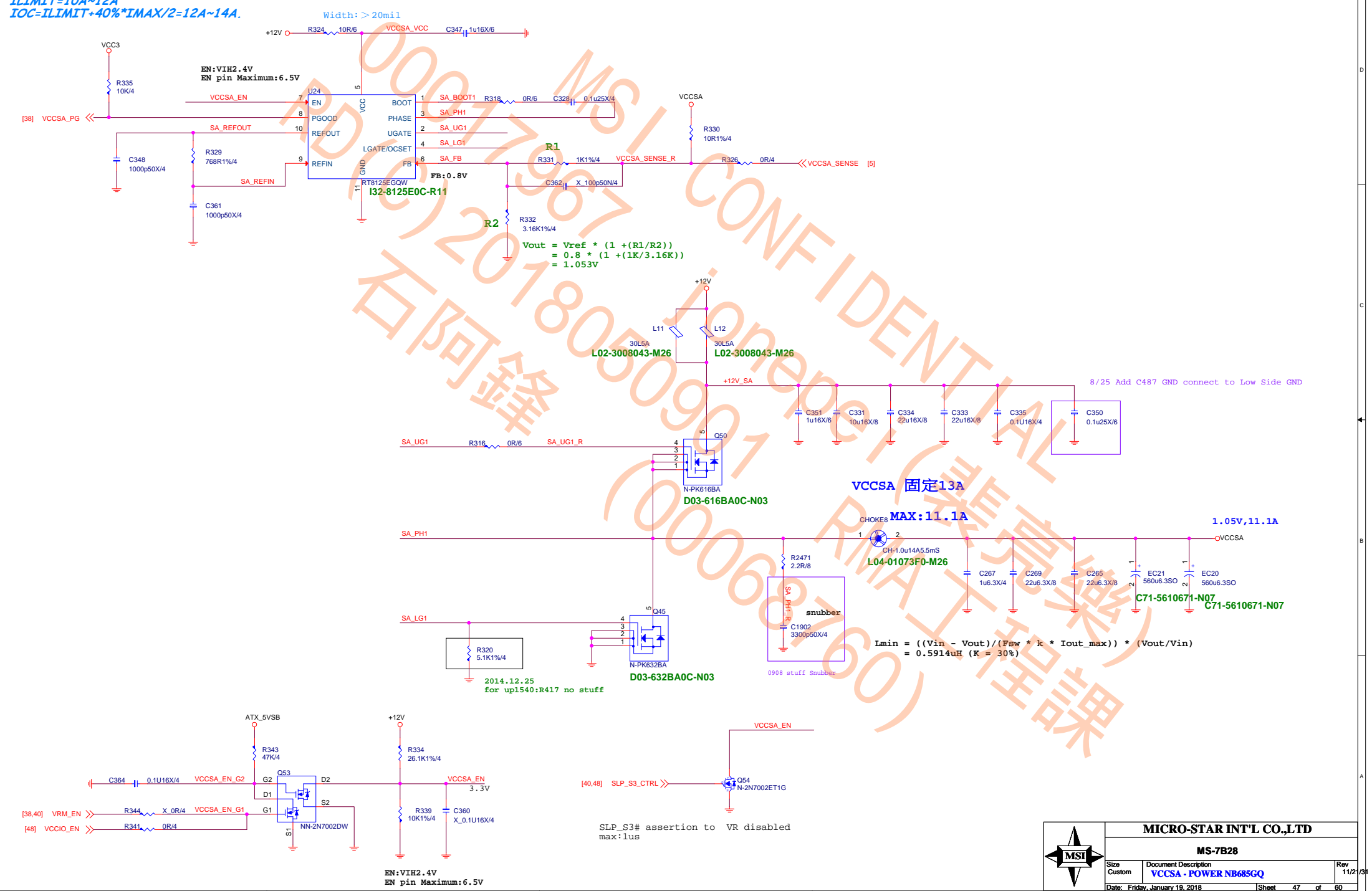


1P8_VSB@1.8V/500mA

2017/1/3 Layout空間不足

VCCSA@1.05V/11.1A

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

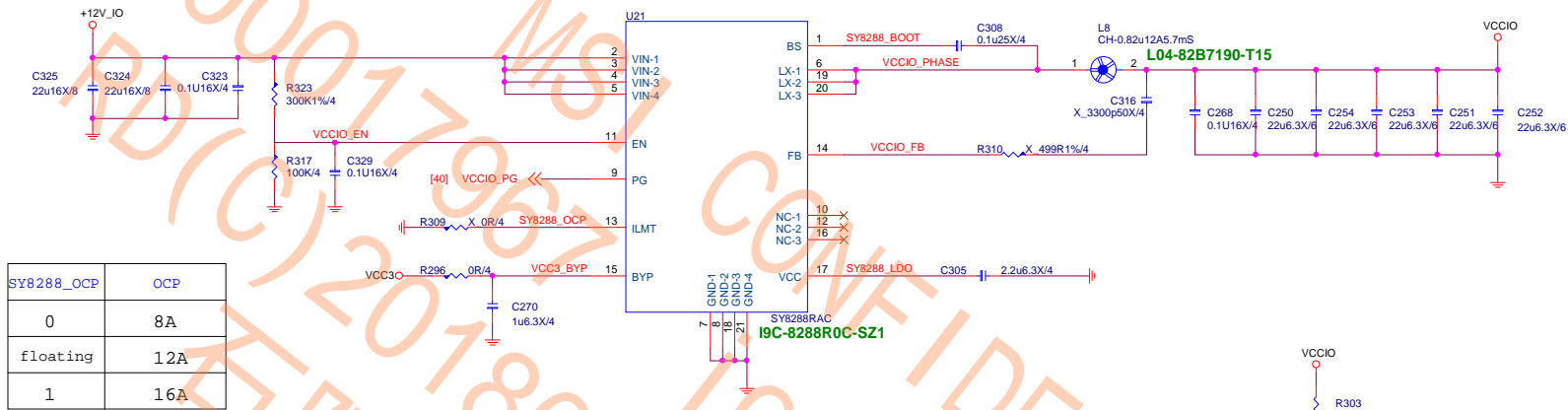
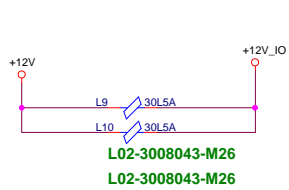


VCCIO@0.95V/6.4A

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

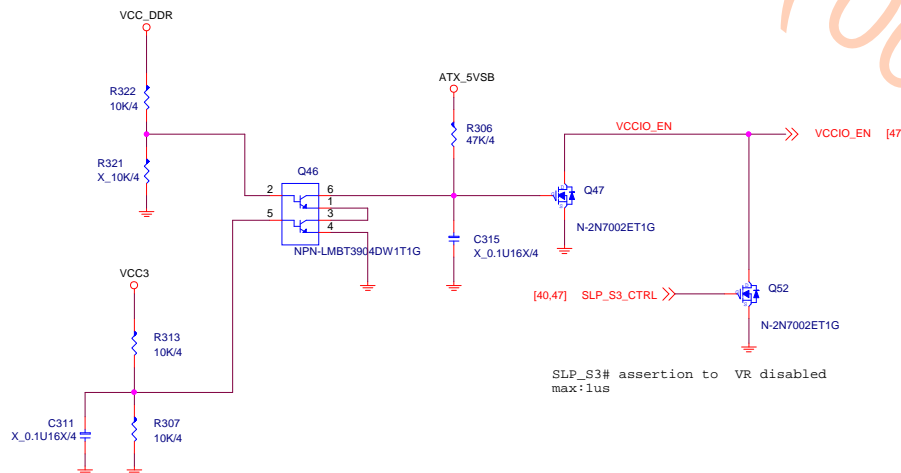
VCCIO 固定12A(floating)

MAX:6.4A

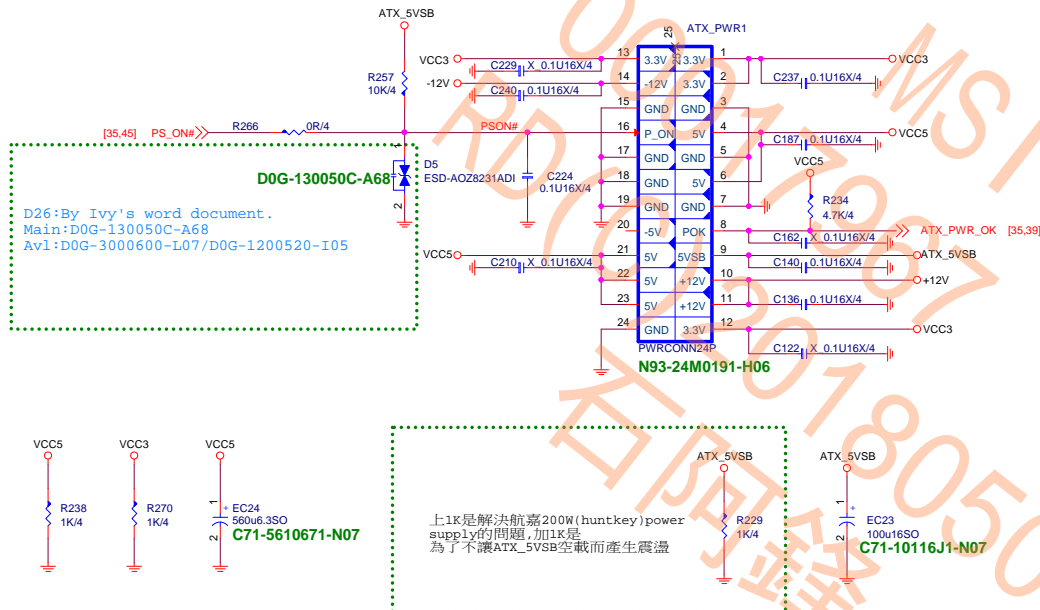


[5] CPU_CNL_N >>> CPU_CNL_N R301 X 5.9K1%/4
CPU_CNL_N come from CPU PROC_SELECT#

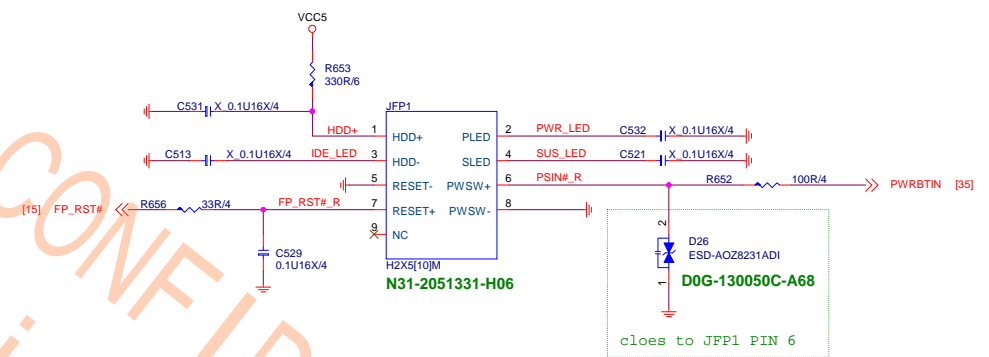
$((1/1.74)+1)*0.6=0.94482$



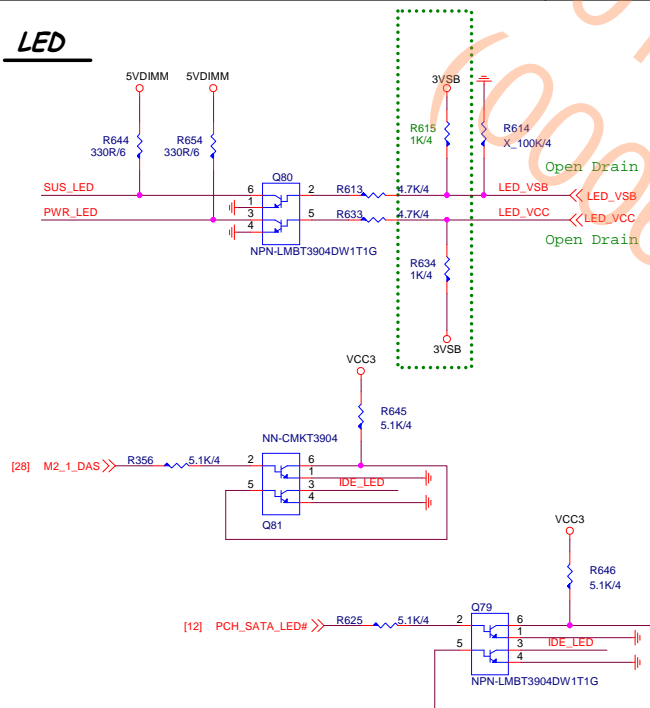
ATX POWER CONNECTOR



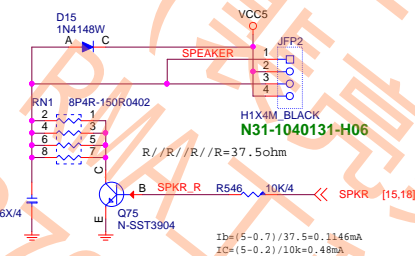
FRONT PANNEL



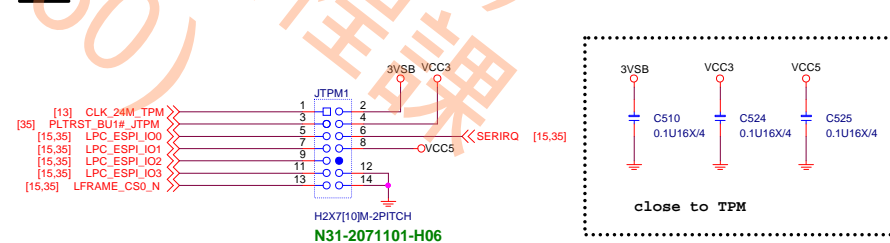
LED



Speaker Pin Header



TPM



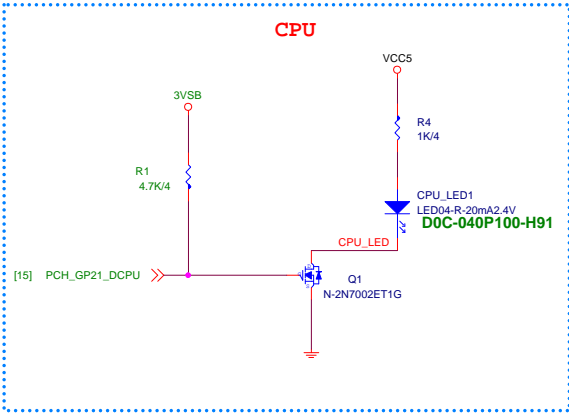
MICRO-STAR INT'L CO.,LTD

MS-7B28

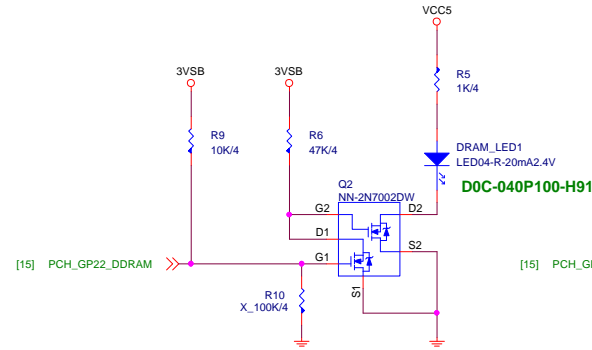
Size	Document Description	Rev
Custom	ATX F_Panel/TPM/MSI_LED	11/2
Date: Friday, January 19, 2018	Sheet 49 of 60	

EZ DEBUG LED

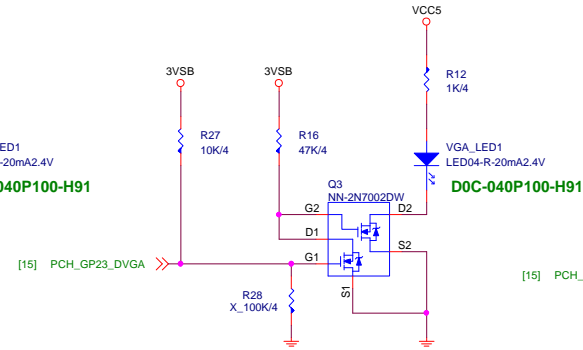
CPU



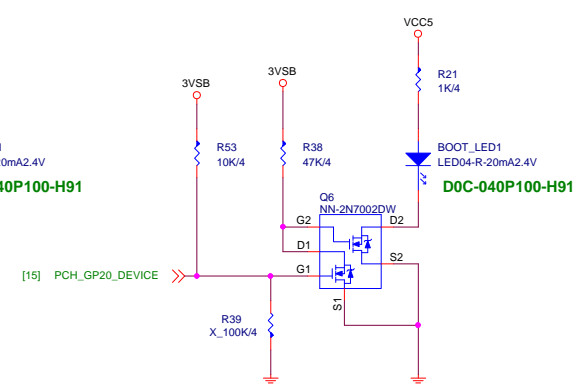
DRAM



VGA



DEVICE



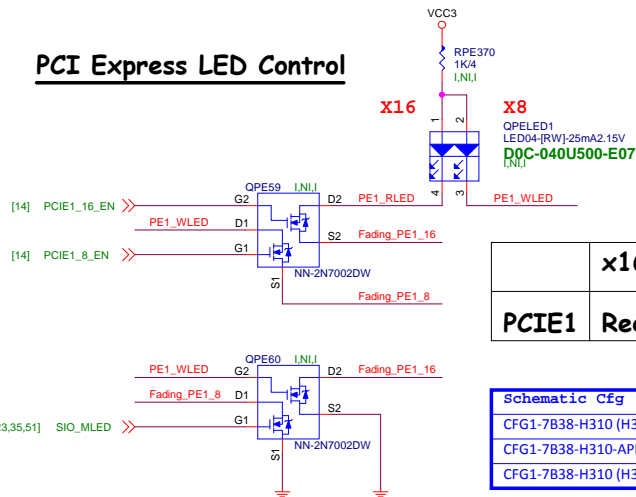
LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

LED

RED:D0C-040P100-H91
AVL:D0C-040S500-E07

WHI:D0C-040T200-H91
AVL:D0C-040S200-E07

PCI Express LED Control



	x16	x8
PCIE1	Red	White

Schematic Cfg	Project	
CFG1-7B38-H310 (H310M GAMING PLUS) ver.1.0	V	A
CFG1-7B38-H310-APRO (H310-A Pro) ver.2.0	X	B
CFG1-7B38-H310 (H310-A GAMING ARCTIC) ver.3.0	V	C

關機斷電狀態下，3個LED先維持default全暗，開機通電後：

1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
4. 因此最後正常順利開機後，三個LED燈都是滅掉的。
(系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作)

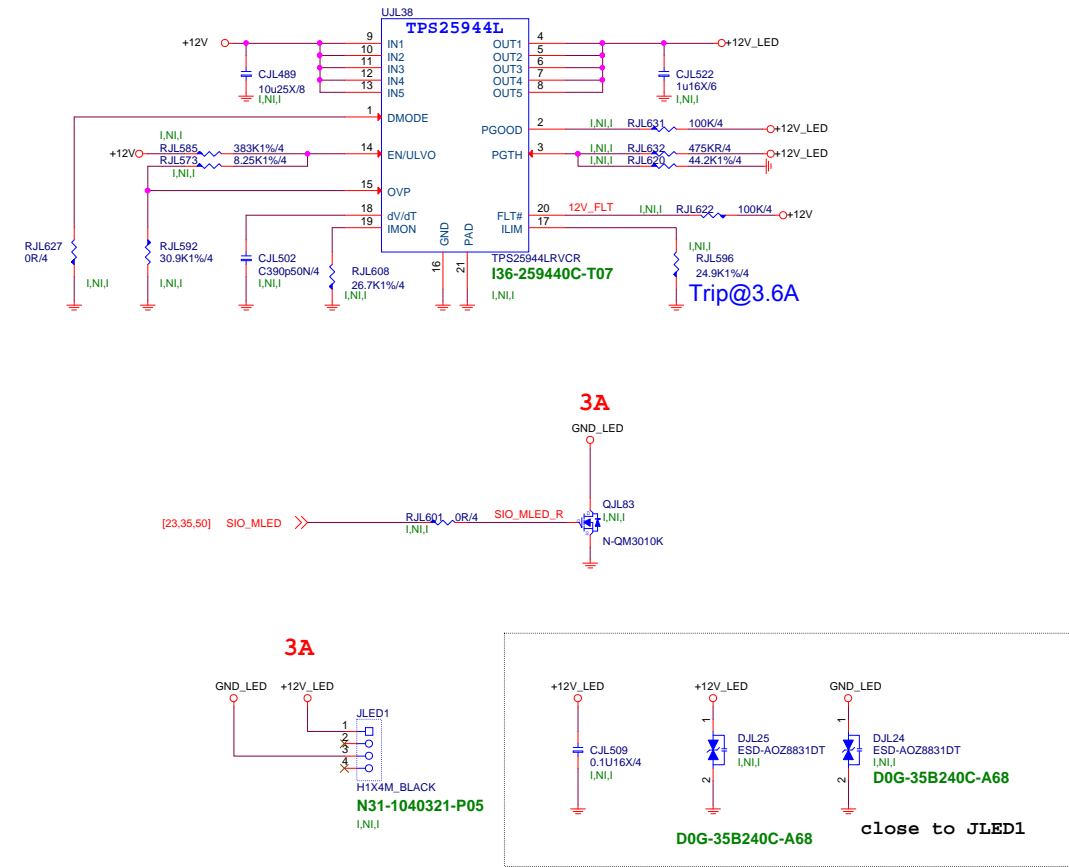


MICRO-STAR INT'L CO.,LTD

MS-7B28

Size	Document Description	Rev
Custom	ALL LED Control	11/2
Date: Friday, January 19, 2018	Sheet 50 of 60	

LED Control by SIO(JLED1)



Schematic Cfg	Project	
CFG1-7B38-H310 (H310M GAMING PLUS) ver.1.0	V	A
CFG1-7B38-H310-APRO (H310-A Pro) ver.2.0	X	B
CFG1-7B38-H310 (H310-A GAMING ARCTIC) ver.3.0	V	C

OPTION BOM PARTS

Schematic Cfg	Project
CFG1-7B38-H310 (H310M GAMING PLUS) ver.1.0	A
CFG1-7B38-H310-APRO (H310-A Pro) ver.2.0	B
CFG1-7B38-H310 (H310-A GAMING ARCTIC) ver.3.0	C

5010 Level

A

EZ Debug LED

O_EZ_GP

LED04-R-20mA2.4V_1608-HF

D0C-040P100-H91

Red

B

O_EZ_PRO

LED04-R-20mA2.4V_1608-HF

D0C-040T200-H91

White

C

O_EZ_GAR

LED04-R-20mA2.4V_1608-HF


D0C-040T200-H91

White

PD0-07B2810-E48

PD0-07B2811-G37

O_PCB_GP




7B28_11

PK0-07B2820-E48

PK0-07B2821-G37

O_PCB_PRO




7B28_21

PS0-07B2830-E48

PS0-07B2831-G37

O_PCB_GAR



7B28_31

5020 Level

A

AUDIO LED

O_AUDLED_GP

LED04-BR125mA2.35V

D0C-040S600-E07

Red

B

O_AUDLED_PRO

LED04-BR125mA2.35V

D0C-040S600-E07

C

O_AUDLED_GAR

LED04-W-20mA3.9V_1608-RH

D0C-040T300-H91

White

60 Level

A

REAR U3

O_REARU3_GP

USB_C1_24_2

N53-18M0201-L06

B

O_REARU3_PRO

USB_C1_24_2

N53-18M0091-F02

C

O_REARU3_GAR

USB_C1_24_2

N53-18M0201-L06

O_DDRSLT_GP

DDRIV_D288

N13-2880681-L06

DDR Slot

O_DDRSLT_PRO

DDRIV_D288

N13-2880561-L06

O_DDRSLT_GAR

DDRIV_D288

N13-2880521-L06

O_PCIE16_GP

SLOT-PCI164P_RED-2PITCH-RH-1

N11-1641671-L06

PCIEx16 Slot

O_PCIE16_PRO

SLOT-PCI164P_BLACK-2PITCH-RH-38

N11-1641221-L06

O_PCIE16_GAR

SLOT-PCI164P_WHITE-2PITCH-RH-4

N11-1641601-L06

O_VGA_GP

DVI24P_BLACK-RH-17

N5B-24F0771-EB6

DVI

O_VGA_GAR

DVI24P_BLACK-RH-17

N5B-24F0771-EB6

O_VGADVI_PRO

VGA_DVI-RH-31

N58-39F0371-EB6

VGA+DVI

O_LA_GP

B310

Lable

MKT

G51-M1SPM62-Q13

PACK LABEL

O_LA_PRO

B310

Lable

MKT

G51-M1SPM61-Q13

O_LA_GAR

B310

Lable

MKT

G51-M1SPM60-Q13

O_PHSK_GP

HS-0409490

E31-0409490-K08

PCH Heatsink

O_PHSK_PRO

HS-0409430

E31-0409430-K08

O_PHSK_GAR

HS-0409520

E31-0409520-K08

O_CHSK_GP

CPU

鐵座

CPU_H1

E21-7869020-F02

CPU Heatsink

O_CHSK_PRO

CPU

鐵座

CPU_H1

E21-7869020-F02

O_CHSK_GAR

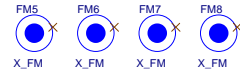
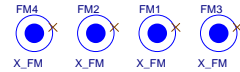
CPU

鐵座

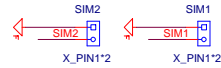
CPU_H1

E21-7A45010-L06

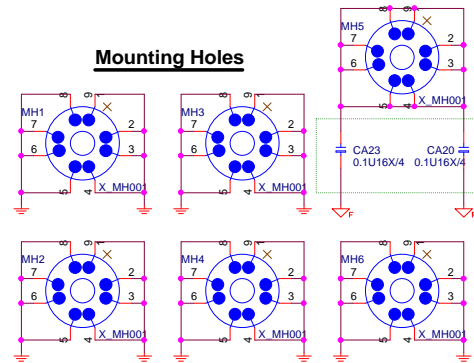
Optical Fiducial Marks-120



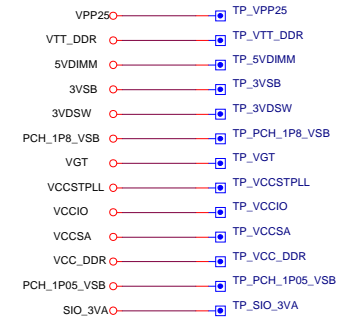
Simulation



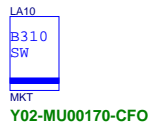
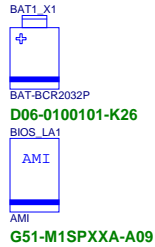
Mounting Holes



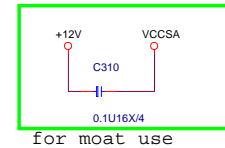
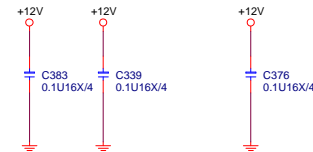
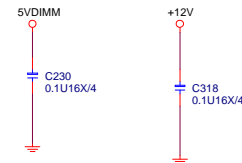
HOLES_4S



Near SIO CHIP



return path



for moat use

For M2 reference +12V USE
please close to under M2